CONTRIBUTED PAPER

Signal Processing and Coding Techniques for 2-D Magnetic Recording: An Overview

This article provides a wide overview of 2-D magnetic recording technology, channel models and capacity, signal processing algorithms, and error-correcting codes attuned to 2-D channels.

By Shayan Srinivasa Garani, *Senior Member IEEE*, Lara Dolecek, John Barry, *Senior Member IEEE*, Frederic Sala, and Bane Vasić, *Fellow IEEE*

ABSTRACT | Two-dimensional magnetic recording (TDMR) is an emerging storage technology that aims to achieve areal densities on the order of 10 Tb/in^2, mainly driven by innovative channels engineering with minimal changes to existing head/media designs within a systems framework. Significant additive areal density gains can be achieved by using TDMR over bit patterned media (BPM) and energy-assisted magnetic recording (EAMR). In TDMR, the sectors are inherently 2-D with reduced track pitch and bit widths, leading to severe 2-D intersymbol interference (ISI). This necessitates the development of powerful 2-D signal processing and coding algorithms for mitigating 2-D ISI, timing artifacts, jitter, and electronics noise resulting from irregular media grain positions and read-head electronics. The algorithms have to be eventually realized within a read/write channel architecture as a part of a system-on-chip (SoC) within the disk controller system. In this work, we provide a wide overview of TDMR technology, channel models and capacity, signal processing algorithms (detection and timing recovery), and error-correcting codes attuned to 2-D channels. The innovations and advances described not only make TDMR a promising future technology, but may serve a broader engineering audience as well.

KEYWORDS | 2-D intersymbol interference channels; 2-D signal processing; coding techniques; magnetic storage; read write channels; systems architecture

I. INTRODUCTION

Modern data storage technologies must balance two conflicting demands: massive storage density and efficiency in design, implementation, and production. Increasing density often requires expensive choices such as switching recording technologies or introducing a new storage medium; moreover, there are diminishing returns involved when approaching the capacity limits of a particular medium. On the other hand, relying on efficient existing technologies mandates lower density, so that the cost per bit is not significantly decreased.

Two-dimensional magnetic recording (TDMR) is one of the most promising candidates among emerging storage technologies, providing a balanced solution to these challenging demands. TDMR allows for very dense storage, while also reusing existing head/media designs from extant forms of magnetic media. TDMR achieves these goals by offering a novel approach: rather than a new medium or a novel head, TDMR relies on significant improvements to signal processing and coding to offer densities beyond 4 Tb/in^2 [1].

TDMR is a novel recording technology driven from a purely signal processing and systems perspective unlike other proposed technologies, such as bit-patterned media (BPM), microwave-assisted magnetic recording (MAMR), and heat-assisted magnetic recording (HAMR). HAMR

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S. S. Garani is with the Electronic Systems Engineering Department, Indian Institute of Science, Bengaluru 560012, India (e-mail: shayangs@iisc.ac.in).

L. Dolecek and **F. Sala** are with the Department of Electrical Engineering, University of California Los Angeles, Los Angeles, CA 90095 USA (e-mail: dolecek@ee.ucla.edu; fredsala@gmail.com).

J. Barry is with Georgia Institute of Technology, Atlanta, GA USA (e-mail: john.barry@ece.gatech.edu).

B. Vasić is with the Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ USA (e-mail: vasic@email.arizona.edu).

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requires the development and production of very specialized write heads. BPM relies on a highly ordered medium, requiring careful lithography. TDMR on the other hand can work with random grains, extending over the current perpendicular magnetic recording (PMR), and providing additive gains over BPM and HAMR.

Naturally, TDMR's advantageous features also come at a cost. In TDMR systems, a very small number of magnetic grains are used to store a single bit, while the write head remains larger, resulting in high intersymbol interference (ISI). TDMR can also suffer from other issues, including, for example, timing problems, jitter noise, electronic noise, and others. Mitigating these problems has led to the development and application of powerful signal processing and coding theory algorithms. Progress in research problems inspired by the challenges of TDMR can offer benefits in many areas.

A. Data Storage Trends

The amount of data being generated each year continues to grow, and this trend shows no signs of stopping. Recent estimates of the total amount of data (the "global datasphere") in 2025 reach 163 zettabytes (ZB), compared to 16 ZB for 2016 [2]. This enormous growth has fueled the demand for larger, denser, and cheaper data storage devices.

One particular area of exploding demand for hard disk drives is the data center, driven by the increasing popularity of uploading data to the cloud. A recent Google position paper notes that YouTube users' uploads currently require one petabyte (one million gigabytes) of additional data storage per day and that the overall trend is exponential [3]. Another area with increased demand for hard drives is cold/archival storage [4].

Naturally, it is desirable to produce drives with larger density in order to meet the increased demand. Today's drives have reached the density of 1 Tb/in^2, but novel solutions are required to reach the next order-of-magnitude improvement. TDMR is among the most promising proposed solutions.

B. Magnetic Memories

Magnetic media are nonvolatile memories that store information by magnetizing a group of one or more magnetic grains; the magnetization is performed by write heads that pass near the surface of the magnetic material. Similarly, read heads detect the current magnetization.

Magnetic media have a long and prominent history in the data storage domain. They date back to the late 19th century inventions of Oberlin Smith and Valdemar Poulsen; the latter used piano wire as the magnetic material [5]. Magnetic tapes were developed in the 1920s and began to find use as part of computer storage in the 1950s. Magnetic storage drives have experienced continuous innovation since then, decreasing in size while improving capacity. Modern drives offer areal densities eight orders of magnitude larger compared to the initial drives of the 1950s such as the IBM 350 [5].

Commercial disk drives used longitudinal magnetic recording (LMR), where the data elements are organized parallel to the recording surface, until the early 2000s. In order to continue increasing areal density despite the superparamagnetic effect, perpendicular magnetic recording (PMR) was introduced in the mid-2000s, although PMR systems were studied by research labs since the 1970s [6]. In PMR systems, the data elements are placed perpendicular to the recording surface, allowing for a denser packing.

Although commercially successful in the last 15 years, PMR-based systems also suffer from an areal density limit around 1 Tb/in^2 [7]. The desire to exceed this density level has led to research into novel forms of magnetic media, including HAMR, BPM, and TDMR.

C. Magnetic Materials

Magnetic materials allow for nonvolatile data storage by enabling a system with two different states, capable of being switched back and forth. The switching (i.e., writing) occurs through magnetic hysteresis, where an external magnetic field is applied to the underlying material, which remains magnetized after the removal of the field. The magnetic reader is capable of detecting the magnetization direction.

The media used in magnetic recording consists of several layers. One of these is the recording layer consisting of the magnetic grains themselves. Various materials for recording layers have been proposed; in the case of the currently popular PMR technology used for 1-D magnetic recording, Co alloys such as CoCr, CoCrPt, CoCrNb, and CoCrTa have been proposed as early as the 1970s. Other layers [e.g., intermediate layers, the soft magnetic underlayer (SUL), adhesion layers, and substrates] are used to improve the signal-to-noise ratio and to protect the recording layer [6].

D. State-of-the-Art Industrial Research

In the magnetic storage industry, array-reader-based magnetic recording (ARMR) [8], [9] schemes are being currently explored toward areal densities in the 1–2 Tb/in^2 regime. In ARMR, multiple read-back streams from an array of readers are captured. The stacked readers have a cross-track separation (CTS) of about 100 nm. Joint signal processing that includes a core 2-D equalization, followed by timing and 1-D detection using a hardware acceleration platform are done to get improved bit error rates. In a recent work [8], dual-reader ARMR performance was evaluated by considering skew-induced variation in the CTS between the two read sensors. Based on bit error rate scan along the cross-track under various squeezed recording and skew conditions, a 5%–10% increase in

squeeze-to-death margin-based areal density gains were predicted over a single-reader for CTS less than 0.6 track pitch. Most recently, Zheng *et al.* [9] have presented an electronic servoing scheme that estimates the location of the dual reader on a per-fragment basis within a zone. This information is used to transform the reference equalizer to a new equalizer that is matched to the estimated location, thereby, sensitive to track misregistration (TMR) effects that equalization is prone to.

In order to realize the full power of TDMR, one needs to eventually go toward a native 2-D paradigm comprising coding and signal processing units to overcome 2-D interference and noise with shrinking tracks and bit lengths.

E. Organization of the Paper

This paper is organized in the following way. In Section II, we present a high-level overview of TDMR technology, including the motivation for its development, along with system requirements, the magnetic materials used, and recording processes. Afterwards, in Section III, we consider TDMR channel models, capacity, and estimates of areal density. In Section IV, we begin with a discussion of signal processing for TDMR based on shingled systems, including single-track and multitrack detection, along with timing recovery. In Section V, we continue with the signal processing aspects of TDMR within a true 2-D framework, beginning with a discussion of the timing recovery problem and continuing toward the problem of detecting an array of bits through a 2-D joint timing recovery and detection scheme prior to error correction decoding. Section VI is concerned with error-correcting code design and optimization, focusing in particular on low-density parity-check (LDPC) codes for TDMR along with some channel specific considerations and coding architectures. Afterwards, we conclude the paper with a few perspectives.

II. TDMR TECHNOLOGY

A. Motivation

A widely held view suggested that conventional recording would not exceed a density limit of 1 Tb/in^2 [10], due to the limiting factor of thermal stability. The challenge of bypassing this supposed limit motivated research into technologies such as HAMR and BPM, but such developments require a total redesign of the medium and read/write heads. Write/read heads are separate devices that are designed independently, and typically can have very different physical widths. The desire to continue using conventional media with possibly array heads, while attaining an areal density of 1 Tb/in^2, motivated the introduction of 2-D magnetic recording in a seminal paper by Wood *et al.* [10] in 2009. Since then, a significant amount of research has been devoted to TDMR.

B. TDMR Recording Theory and Principles

TDMR technology can be seen as an extension of PMR technology, itself having improved on the previous standard of longitudinal recording. The main difference between TDMR and PMR is the fact that a single bit is stored in a very small number of grains, and, as a result, the head is larger than the tracks, resulting in overlapping tracks during writing. This effect is known as shingling.

1) Recording Physics Overview: In traditional magnetic recording systems, writing is performed by sweeping the write head from left to right until a track is entirely written; afterwards, the head is moved down to the next track, and the process continues. The writing process consists of magnetizing (a large number of) grains in the medium. Reading is performed by producing a signal waveform; this waveform is then used to reconstruct the data. An illustration of this process is shown in Fig. 1(a). On the other hand, with TDMR systems, the data are not organized as a series of well-separated tracks, but rather in a 2-D array; moreover, the number of grains representing a bit is much smaller, and, as a result, the magnetic head is larger than the tracks which contributes to overwriting. Magnetic grains/domains are irregular and not necessarily confined to bit boundaries, leading to partial erasures while writing an adjacent cell. Reading, as shown in Fig. 1(b), is done by sensing the magnetization and convolving it with the read-head response, followed by a sampling procedure at the bit centers.

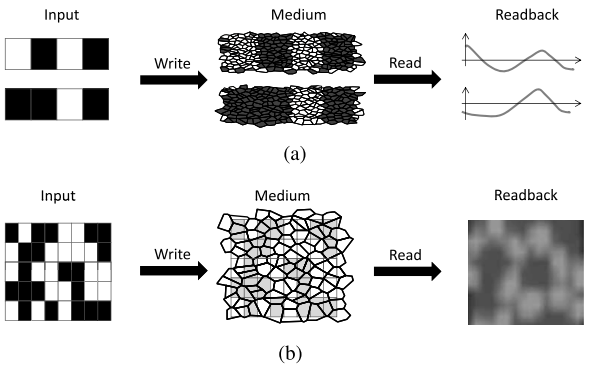


Fig. 1. ***Conventional and TDMR write/read processes. In a conventional system (a), the write head is moving from left to right (down-track) until the first track is written, and then is moved (down) to the second track, etc. The result of writing data [shown as black (+1) and white (–1) squares] is a sequence of bits composed of many magnetized grains (shown as black and white areas or irregular shapes). A read-back process produces a signal waveform used to reconstruct the data. In a TDMR system (b), the data are organized in a 2-D array. The grains on a medium are comparable in size to bits and their positions and shapes are random. The 2-D read-back signal is a result of sensing magnetization of the media by the read head. The sampled read-back signal is obtained by convolving the magnetization of the medium with the response of the read head and then sampling them at bit centers.***

2) Recording Effects from Channels Perspective: As previously described, in TDMR, the write head exceeds the size of the track, so that write sweeps (partially) overlap. Data are thus stored in a 2-D array, and reading suffers from 2-D ISI. In order to reflect these effects, TDMR channel models have a higher complexity. These models are discussed in the following section.

C. System Requirements and Considerations

The promise of TDMR systems is to build on the existing magnetic recording backbone without requiring significant, expensive breakthroughs in materials or head design. Existing physical technology is reused, resulting in significant challenges that must be answered. These challenges must be addressed in order to meet critical performance requirements (e.g., areal density, latency, reliability).

In particular, TDMR reuses the same head as a traditional 1-D magnetic recording system, but allows the tracks to be narrower than the write head, resulting in so-called shingled writing. (We note that the read and write heads can be of different widths, as they are independently designed.) In shingled writing, each sweep of the write head partially overwrites previous tracks. The result is significant interference both along and across tracks. Dealing with this interference requires novel innovations in signal processing and coding algorithms.

One of the challenges of shingled writing is the fact that each individual track written affects other tracks (due to the fact that the write head is larger than the track width), so that overwriting a single track is not possible without corrupting other tracks. That is, in-place updates are made more difficult in shingled recording systems, including TDMR.

Shingled recording systems group together contiguous tracks into bands; data can be appended to (but not rewritten in) each band. A number of tracks are reserved between each band, allowing for appending additional writes. There are several choices for managing bands. One approach is to organize each band as a circular log, moving the current data at the tail to the head and using the now-free areas. A second choice is to compact fully written bands into a fewer unused bands. Another solution involves using a log-structured file system (LFS). Recent research [11] has focused on developing these solutions in order to efficiently enable in-place writes. A related concern involves integrating shingled systems into a general storage system, requiring potential changes to file systems.

This concludes our high-level overview of TDMR. We are now ready to discuss TDMR channel models and the related tasks of estimating TDMR capacity and areal density.

III. CHANNEL MODELING, CAPACITY, AND AREAL DENSITY ESTIMATION

This section is concerned with TDMR channel models, the capacities of these channels, and the estimation of areal density. The section is organized as follows. We begin by discussing a hierarchy of channel models for TDMR, starting with low-complexity and low-accuracy models and progressing toward higher complexity, high-accuracy channels. Afterwards, we focus specifically on the Voronoi-based model and discuss the details of this channel model (media model, read and write procedures, and noise characteristics) in depth. The following sections are concerned with estimating the main characteristic of these channels, i.e., the channel capacity under stationary ergodic conditions, culminating in the estimation of the mutual information rate over the Voronoi channel model in Section III-F. Finally, we apply these concepts to optimize the Voronoi channel bit aspect ratio (BAR). Throughout we leverage information-theoretic tools, e.g., entropy, mutual information, mutual information rate (MIR), along with notions from probabilistic graphical models.

Unlike today's recording systems, the approach in TDMR systems is to store one bit in as few grains as possible on a conventional magnetic media. To ensure a sufficiently large magnetization field capable of magnetizing materials with high coercivity, the head is made larger than the track width. However, to achieve a higher areal bit density, the tracks should be very narrow. As a result of narrower tracks, each sweep of the head during writing partially overlaps with the previous track [10], [12]. As opposed to the traditional systems where data are organized in well-separated tracks [shown in Fig. 1(a)], in TDMR systems, the data are arranged in a 2-D array [Fig. 1(b)]. In traditional systems the intertrack interference is small, and the only severe source of noise was ISI along the track which is controlled by a sequence detector. In TDMR system, the head picks up magnetization from adjacent tracks. Consequently, there is severe ISI both along a track and across the tracks as the head is much larger than the physical dimensions of a stored bit [13], [14]. Narrow read heads can be fabricated (minimizing ITI) though there is an inevitable penalty in head noise. Often, the lithography at these dimensions becomes more difficult [15]. The 2-D read-back signal shown in Fig. 1(b), obtained from a typical recording medium, illustrates this severity. Several channel models are proposed to aid simulations in studying coding and signal processing algorithms. These models vary in complexity and accuracy in capturing the behavior of a magnetic medium.

A. Overview of Hierarchy of Channel Models

In this section, we introduce the most commonly used channel models for TDMR systems. We classify these channel models into: 1) binary error and erasure models; 2) discrete grain models; 3) Voronoi media models; and

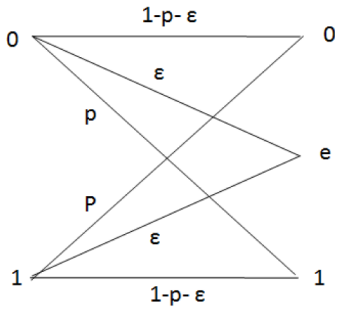


Fig. 2. ***The representation of binary error and erasure channel model.***

4) micromagnetic media models in the increasing order of accuracy and computational complexity. In binary error and erasure models, the error in the write/read-back process is modeled as a binary input channel where bits are either erased, stored incorrectly or stored correctly. Discrete grains models assume that the medium consists of tiles where each tile represents a grain and is chosen from a predefined set of tile shapes. Voronoi models consider the recording medium as a Voronoi tiling of the plane, where each Voronoi region represents a grain and the distribution of Voronoi centers is modeled using a point process. The micromagnetic models simulate the sizes, shapes, and distribution of the grains close to an actual magnetic recording medium. The magnetic domains are formed using the Voronoi regions whose centers are the grain centers.

1) Binary Error and Erasure Model: This model is the simplest among all of the proposed models for TDMR channels [16], [17]. As shown in Fig. 2, a TDMR channel is modeled as a binary input channel where bits are either erased with an erasure probability ϵ, stored incorrectly with a probability p or stored correctly. This model is memoryless and does not take into account that adjacent bit errors can influence a current bit. Although this channel model cannot capture the effects of correlated error events in TDMR systems, it is beneficial for the design and evaluation of error-control codes and decoders for TDMR systems at a first pass.

2) Discrete Grains Model: The discrete grains model is a simple model for the realization of the grains distribution on a magnetic medium [18]–[20]. In the discrete grains model, grains are assumed to be chosen from a set of shapes, and the magnetic medium is considered as a 2-D array which is tiled by these predefined shapes. In [21], Kavcić *et al.* introduced a relatively simple 2-D magnetic grains model of the TDMR channel where grains on the medium are one of four rectangular tiles from the set of 1×1, 1×2, 2×1, and 2×2 rectangular tiles. Fig. 3 shows the four grain types. The magnetic medium is considered as a rectangular grid where each cell represents a channel bit. The write head writes at the centers of cells in a row-by-row fashion, and the grain which contains the cell is magnetized. As the

Fig. 3. ***The set of four rectangular tiles: 1 × 1, 1 × 2, 2 × 1, and 2 × 2 considered in the 2-D discrete grain channel model introduced in [21].***

cell (channel bit cell) size can be smaller than the grain size, a grain can be overwritten several times during the write procedure. The magnetization of grain is considered to be the magnetization which is polarized last onto one of cells containing the grain. For instance, if the magnetization process is performed in a row-by-row fashion starting from the top-leftmost cell of the medium and ending in the bottom-rightmost cell, then the magnetization of each grain would be the magnetization of its bottom-rightmost constituent cell. As a result of this phenomenon, some of the input bits cannot be recovered from the read-back signal [22], [23]. Fig. 4 shows a realization of discrete grain channel based on the aforementioned write process. The magnetic head does not have any preliminary information during the read-data process about the arrangement of tiles on a medium, so that the head assumes that the medium is composed of 1×1 tiles only. However, this model is not realistic from a fabrication perspective, although useful for channel abstraction purposes.

3) Voronoi Grain Model: The Voronoi grain models consider the magnetic medium as a tiling of Voronoi regions, where each Voronoi region represents a grain. Each Voronoi region is identified based on the distribution of the grain centers, i.e., the nucleus of the cell. Here, we present two approaches for generating a random Voronoi tiling. In the first approach, the grain centers are distributed as random deviations from their ideal positions, where the ideal positions are the center of each cell of a rectangular grid. The randomness in the shape and position of grains is modeled by shifting the grain centers randomly from the cell centers [24], [25]. In the second approach, the grain centers are generated with the Poisson-disk distribution using the boundary sampling method described in [26]. and used in [27]. The distance between two grain centers are restricted to be more than

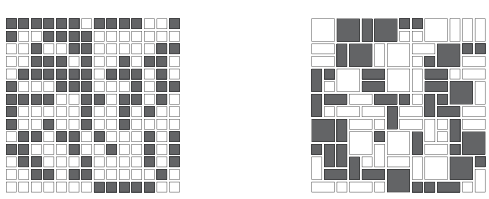


Fig. 4. ***(a) Ideal medium of size 14 × 14. (b) Example of a medium consisting of grains of sizes up to 2 × 2 cells.***

a predefined parameter, the center-to-center (CTC) distance. Furthermore, each new grain should at least touch one of the existing grains to obtain a closer random packing with respect to the CTC constraint. Specifically, let N_g be the number of grains on the medium with the coordinates $(x_i, y_i) : i = 1, 2, \ldots, N_g$. The medium is partitioned into a rectangular grid where each rectangle cell represents a bit area. The length and width of the bit area in the down-track and cross-track directions are determined by the bit-length (BL) and track-width (TW) parameters. Therefore, the number of grains per bit cell area can be identified; this number depends on the CTC parameter and the length and width of the bit cell area. The number of grains per bit cell area contributes to the grain density on the medium. The second approach is a more accurate description of the medium than the first method. Fig. 5 shows an instance of the Voronoi-based magnetic medium. The magnetic head during the read/write processes does not have any advance knowledge of the grain positions, sizes, and shapes on the magnetic medium. Therefore, the magnetic head assumes that the bit cells are in the form of rectangles. Fig. 6 shows an instance of writing on the Voronoi-based media model. Each rectangular cell of size $B_x \times B_y$ and represents a channel bit. B_x and B_y represent the size of each bit in the cross-track and down-track directions. When a bit is written into the medium, all grains whose centers lie within the bit region are polarized according to the bit value. We can also consider overwrite effects within a track and across the tracks represented by the grain flip probability (GFP) parameter [27]. The overwrite effects depend on the write order and the design of read/write head. When the bit value at current position (i, j) differs from either of the two neighboring bits, i.e., $(i, j + 1)$ and $(i + 1, j)$, each grain in the current bit region can flip its polarity with a GFP. If the two neighboring bits have the same bit values as the current bit, then there are no write-in errors in the current bit region. The discrete read-back signal is obtained by convolving the magnetization of the medium with the read-head response and then sampling at cell centers. Fig. 7(a) and (b) shows the magnetization of an ideal and the actual medium, respectively.

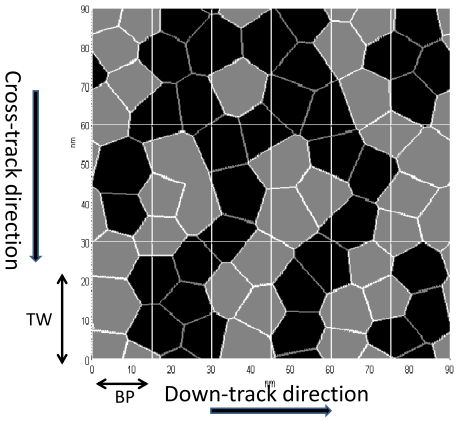


Fig. 5. ***An example of the Voronoi channel model for a TDMR system. We set the length of each bit cell in the horizontal (down-track) direction to be BP= 15 nm and in the vertical (cross-track) direction to be TW= 30 nm. The CTC parameter is considered to be 10 nm.***

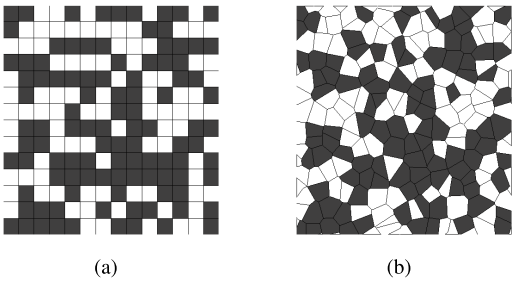


Fig. 6. ***Writing on the Voronoi-based media model (first method). (a) The resultant magnetization of an ideal medium. (b) The resultant magnetization of an actual medium. The grains with magnetization +1/ − 1 are colored white and black, respectively.***

4) Micromagnetic Model: Micromagnetic models accurately define each process involved in modeling the channel and are suitable for optimizing head characteristics and media dimensions [28]–[31]. However, its high complexity makes it unsuitable for developing and studying various signal-processing and error-correction coding algorithms [32], [33]. The micromagnetic recording model assumes a granular thin film medium in which grains are uniformly magnetized. This model makes no prior assumptions of a grain shape or location. The magnetostatic and exchange interactions between nearest neighbors are calculated taking full account of the grain shape, and the magnetostatic interactions between more distant pairs of grains are computed hierarchically. The time evolution of the magnetization is computed by integrating the Landau–Lifshitz–Gilbert (LLG) equation in spherical polar coordinates using a Krylov ordinary differential equation (ODE) solver [34]. Head-field distributions are externally precomputed for some direct currents (dc), and the recording sequence is defined by the

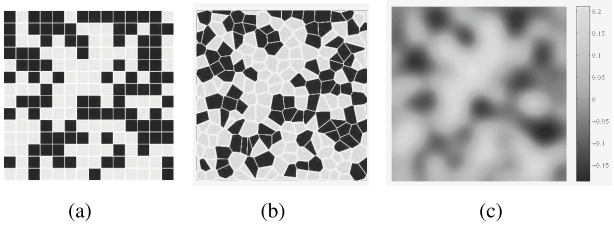


Fig. 7. ***Write/read model for the Voronoi medium. (a) Desired magnetization of an ideal medium. (b) Magnetization of a nonideal medium. (c) Read-back signal (before sampling). We assume the read-back impulse response to be a truncated 2-D Gaussian pulse of unit energy with half-maximum of 1 bit-period and a span of 3 bit-periods in both dimensions.***

velocity of the head and a head current waveform represented by the random bit sequence to be recorded. The field at each point of interest in the medium is then computed by spatially interpolating the head-field distribution.

We also note that there are intermediate channel models between the Voronoi and the micromagnetic model which replace the LLG dynamics with a binary switching process, but still include demagnetization fields with exchange coupling [32].

B. The Voronoi Model and Physical Relevance

Voronoi-based media models give a good tradeoff between implementation complexity and the accuracy of representing a magnetic medium. Voronoi channel models typically involve three components: 1) media model: models the distribution of grain centers on the medium; 2) write process: models the magnetization process of grains while writing data onto the magnetic medium; and 3) read process: models the process of reading back data from the magnetic medium. In the following, we introduce the details of this model.

1) Recording Media Model: The Voronoi tiles are used to simulate the irregularities of magnetic grains. A grain is defined as the smallest region on the magnetic medium that can be independently magnetized, i.e., the smallest magnetic domain. The distribution of grains on the medium can be modeled using a Poisson-disk process with boundary sampling, as proposed in [26]. Each new grain is randomly generated such that it touches at least one of the existing grains to achieve a close random packing under the CTC constraint. Before a new grain is generated, the boundary that is at a distance of CTC from the existing grain centers is identified. The position of a new grain is randomly generated with uniform probability density on the identified boundary.

The recording medium can be viewed as the Voronoi tiling of the shifted grain centers with their regions representing the grains. The medium is split into a rectangular grid, where each rectangular cell of size BL × TW represents a channel bit, where:

- bit length (BL) denotes the length of bit cells in the down-track direction;
- track width (TW) denotes the length of bit cells in the cross-track direction.

The BAR is defined as $\text{BAR} = \frac{TW}{\text{BL}}$. We note the physical significance of this parameter. The act of writing and reading an information bit from a bit cell, i.e., from a rectangular cell with a given bit length and BAR constitute an instance of a noisy communication process, i.e., a noisy channel. The bit cell area is equivalent to the channel bandwidth. The channel bit density (CBD) is given by

$$\text{CBD} = \frac{1}{\text{TW} \times \text{BL}} \text{ coded bits/unit area.} \tag{1}$$

2) Write Process: During the writing process, the head writes the symbol $x_{i,j} \in \{-1, 1\}$ onto the medium by changing the magnetic polarity of all grains whose centers lie within the (i, j)th bit cell according to the value of bit $x_{i,j}$. Magnetic domains are formed by the continuous regions of Voronoi cells with the same polarity of magnetization. The channel input signal $x(t_1, t_2)$ is

$$x(t_1, t_2) = \sum_i \sum_j x_{i,j} \Pi_{\mathbf{TW}}(t_1 - i \times \mathbf{TW}) \Pi_{BL}(t_2 - j \times \mathbf{BL}) \tag{2}$$

where $x_{i,j} \in \{-1, +1\}$ is the symbol which will be written on the (i, j)th bit cell and

$$\Pi_T(t) = \begin{cases} 1, & 0 \le t < T \\ 0, & \text{otherwise.} \end{cases} \tag{3}$$

The indices t_1 and t_2 refer to spatial coordinates, i.e., on the magnetic disk.

3) Read Process: The read-back signal is a result of variation in the magnetic flux from the grains on the medium. Hence, the read-back signal depends on the grain distribution, grain magnetization, and read-head design [24]. Let us suppose that the read head picks up magnetization only from $m \times n$ neighboring cells. As a result, the read-head output sample $y_{i,j}$ at the center of the (i, j)th cell depends only on the polarity of the grains in the $m \times n$ neighborhood around the (i, j)th cell, denoted as $C_{i,j}$. We use the 2-D Gaussian pulse model for the read-head sensitivity function. The 2-D Gaussian pulse is characterized by the pulse widths PW50_x and PW50_y at half-amplitude in the down-track and cross-track directions

$$h(x, y) = \frac{\ln 2}{\pi \text{PW50}_x \text{PW50}_y} \exp\left(- \frac{(\ln 2) x^2}{\text{PW50}_x^2} - \frac{(\ln 2) y^2}{\text{PW50}_y^2} \right) \tag{4}$$

with

$$\int_{-\infty}^{\infty} \int_{-\infty}^{\infty} h(x, y)\, dx dy = 1. \tag{5}$$

The read-head sensitivity function is the contribution of each grain toward the generation of a read-back signal. Fig. 8 shows the distribution of grains on the medium, magnetization of the Voronoi regions on the medium, and the continuous time read-back signal without electronic noise.

Let $h_{i,j}[p, q]$ be the discrete-time read response of the bit at position (i, j). The indices p, q are integers representing samples at the 2-D bit rate postsampling. These response coefficients are random and dependent on the position and shape of grains within the bit area. The average bit response is obtained by taking the expectation on these random response coefficients

$$h(p, q) = \mathbf{E}_{I,J}\left[h_{i,j}[p, q]\right] \tag{6}$$

where I and J are random variables indicating the distribution of the positions of grain centers in the down-track and cross-track directions, respectively. Therefore, the above averaging is taking into account all possible grain positions.

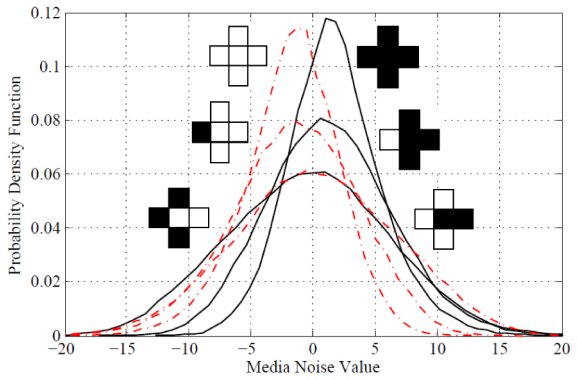


Fig. 8. ***The media noise distribution is shown for different input patterns. For simplicity, the media noise is averaged over the corner bits of the 3 × 3 input region. The white and black squares correspond to −1 and +1 polarization, respectively. The input patterns corresponding to the red (black) curves are on the left (right) side of the curves. The parameters of the Voronoi channel are CTC= 7 nm, BL= 7.5 nm, and TW= 16 nm. It is demonstrated that more transitions result in wider distribution interpreted as more media noise.***

The read-back signal sample without considering the electronic noise is given by

$$y_{i,j} = \sum_p \sum_q x_{i-p,j-q} h_{i-p,j-q}[p,q] \tag{7}$$

where $x_{i,j}$ is the symbol written on the (i,j)th bit cell. Furthermore, the ideal read-head output $s_{i,j}$ is obtained by considering the average discrete-time output of the (i,j)th bit area as

$$s_{i,j} = \sum_p \sum_q x_{i-p,j-q} h[p,q]. \tag{8}$$

The mean squared value of the read-back signal V_p is defined by

$$V_p^2 = \sum_p \sum_q |h[p,q]|^2. \tag{9}$$

The media noise comes from the random perturbations of $h_{i,j}[p,q]$ around the average response $h[p,q]$. Therefore, the variance, or, equivalently, the energy of media noise σ_m^2 is obtained by

$$\sigma_m^2 = \mathrm{E}_{I,J}\left[\sum_p \sum_q |h_{i,j}[p,q] - h[p,q]|^2\right]. \tag{10}$$

Then, we can define three SNRs for a TDMR system according to the above definitions as

$$\mathrm{SNR} = 10\log_{10}\left(\frac{V_p^2}{\sigma_m^2 + \sigma_e^2}\right)$$

$$\mathrm{SNR}_{\mathrm{Media}} = 10\log_{10}\left(\frac{V_p^2}{\sigma_m^2}\right)$$

$$\mathrm{SNR}_{\mathrm{Elec}} = 10\log_{10}\left(\frac{V_p^2}{\sigma_e^2}\right) \tag{11}$$

where SNR is the overall SNR, and $\mathrm{SNR}_{\mathrm{Media}}$ and $\mathrm{SNR}_{\mathrm{Elec}}$ are the SNRs corresponding to the media and electronic noise, respectively.

4) Voronoi Channel Noise Characteristics: Fig. 8 demonstrates the media noise distribution for different input patterns specified close to the curves. For simplicity, the corner bits of the 3 × 3 region are averaged out in generating the distribution histogram. The dashed red curves show the distribution of the input data with inverse polarity resulting in symmetric distributions over the y-axis. Based on extensive simulations [35]–[37], the Voronoi channel media noise distribution is shown to be close to the Gaussian distribution. Thus, media noise distribution can be approximated with the Gaussian distribution with mean and variance dependent on input information such that

$$p(y_{i,j}|x_{C_{i,j}}) = \frac{1}{\sqrt{2\pi\sigma^2_{x_{C_{i,j}}}}} \exp\left(\frac{-(y_{i,j} - s_{i,j} - m_{x_{C_{i,j}}})^2}{2\sigma^2_{x_{C_{i,j}}}}\right)$$

where $m_{x_{C_{i,j}}}$ and $\sigma^2_{x_{C_{i,j}}}$ are the mean and variance of the media noise for the case of input state $x_{C_{i,j}}$.

For the case of ideal medium where the bit cells are in the form of rectangles, under linearity assumptions, the discrete read-head output or "ideal values" $s_{i,j}$ is obtained by cross correlating the magnetization pattern of the ideal recording medium with the read-head impulse response and sampling at the center of bit area in the down-track direction. Jitter noise arises due to interactions of grains at the bit boundaries and is more prominent when the neighboring bits differ from the current bit. Therefore, the characteristics of jitter noise depend on the data patterns written onto the medium. We have analyzed the media noise characteristics for a read-head response of a 2-D truncated Gaussian pulse with 3 × 3 span [25], [38]. Fig. 9 shows the media noise variance for different 3 × 3 input patterns. The media noise variance is greater for the input patterns with more transitions in cross-track and down-track direction. The most harmful input patterns are the ones with consecutive transitions in both cross-track and down-track directions. Therefore, neighboring bit transitions lead to an increased media noise which results in degradation of the detector performance [32], [36], [38].

C. Capacity Estimation and Projected Areal Densities

In Section III-B, we detailed the Voronoi channel model. The following sections are concerned with estimating the capacity of such channels.

The capacity of a data storage system is the upper limit of the number of bits per unit area that one can store on the magnetic medium at an arbitrarily low probability of read-back error. Based on Shannon's channel coding theorem [39], for a given noisy channel with channel capacity C, if we choose a long enough code length n and rate $R < C$, there

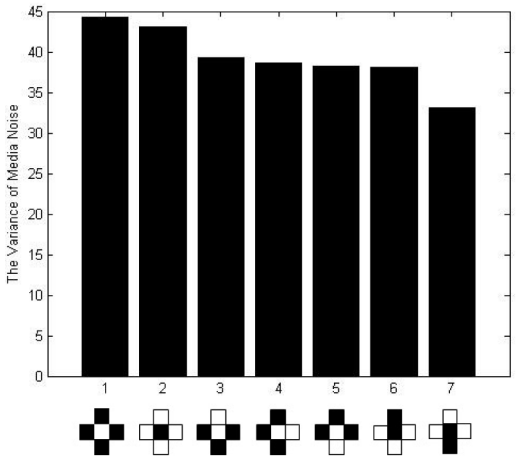


Fig. 9. ***Observation of media noise variance for the Voronoi channel with the parameters CTC =7 nm, BP =7.5 nm, and TW =16 nm. In the 3 × 3 input patterns 0 and 1 are represented by white and black, respectively. It can be inferred that the no isolated bit patterns is one of the harmful patterns for the Voronoi channel [38] Note that the displayed values are based on simulations with a limited number of inputs, explaining the difference between the variance of media noise for the inverse patterns 6 and 7.***

exists a code with probability of error $p_e^{(n)}$ small enough, i.e., there exists an $\epsilon_n > 0$ such that $p_e^{(n)} < \epsilon_n$. If one attempts to write more bits per unit area of medium than the channel capacity, it is not possible to retrieve data with an arbitrarily low probability of error. Therefore, evaluating the channel capacity is important to channel engineers since it provides an upper bound on the code rate of the error-correction code that needs to be utilized [40].

Although the bit error rate is a useful performance metric for optimizing parameters of data storage systems [32], [33], it cannot provide information about the achievable user storage density. The capacity of a data storage system can serve as the ultimate performance benchmark for designing error-correction codes and for simultaneously optimizing parameters of the storage system [41], [42]. Using bit error rate as the comparison criterion encapsulates the channel and the detector as a binary symmetric channel which provides a loose lower bound on the information rate. On the other hand, direct computation of information rate for different input distributions and BARs can be easily translated to the amount of reliably stored bits per magnetic grain and areal density gains [43].

In a recent work [44], Chan *et al.* use the grain-flipping probability model to perform an user areal density optimization together with a software recording channel that is able to include the impact of the generalized partial response equalizer, soft-output Viterbi algorithm detector, and LDPC decoder on the final performance. By varying the bit length, track pitch, and code rate in the simulations, highest user areal density achievable for a given head/medium setup is evaluated empirically. However, the detector is still 1-D.

Let us get into the information-theoretic aspects for the Voronoi channel model. The capacity of discrete channels is defined as the maximum mutual information rate over all discrete-input distributions [45]. Computing the capacity for 1-D and 2-D channels has been one of the main challenges in information theory [45], [46]. Determining the achievable transmission rates of information across noisy channels has been a long-standing open problem. Various bounds, either rigorous [47], [48], numerical [49], [50], or conjectured [51], on the capacity of certain 1-D discrete input channels have been proposed. It is shown that the MIR can be accurately computed using Monte Carlo methods [52]. In [53], information rate is computed for 1-D AWGN channels with memory using the forward recursion of the sum–product [Bahl–Cocke–Jelinek–Raviv (BCJR)] algorithm [54]. As for 2-D channels, Chen and Siegel introduced lower and upper bounds on the estimation of information rate using Monte Carlo methods [55]. In [56], Shental *et al.* used the generalized belief propagation (GBP) algorithm [57] for detection and information rate estimation of 2-D AWGN channels with memory. In [58], Sabato *et al.* used GBP to estimate the capacity of 2-D ISI channels with run length limited (RLL) [59] input sequences.

From an information-theoretic view [55], for TDMR systems, a commonly used channel model is the 2-D finite-state ISI channel with additive white Gaussian noise (AWGN), described by

$$y_{i,j} = \sum_{k=1}^{M}\sum_{l=1}^{N} h_{k,l}x_{i-k,j-l} + n_{i,j} \tag{12}$$

where $xi,j \in \{-1, +1\}$ indicates the magnetization of (i, j)th channel's bit cell, yi,j is the (i, j)th read-back sample, and n i,j is the realization of noise which is a zero mean Gaussian noise with variance $N_0/2$. The mutual information rate (MIR) of the TDMR channel with the probability distribution function $p(\mathbf{y}|\mathbf{x})$ is defined as the mutual information between channel's input $\mathbf{x} = [xi,j]$ and output $\mathbf{y} = [yi,j]$. To put this in a rigorous form, we have

$$\text{MIR} = \frac{1}{NM} I(\mathbf{X};\mathbf{Y}) = \frac{1}{NM} H(\mathbf{Y}) - \frac{1}{NM} H(\mathbf{Y}|\mathbf{X}) \tag{13}$$

where $H(\cdot)$, $H(\cdot|\cdot)$, and $I(\cdot;\cdot)$ are the entropy, conditional entropy, and mutual information functions, respectively. Let us deal separately with the two terms of the MIR. The second term $H(\mathbf{Y}|\mathbf{X})$, the entropy of noise, can be computed analytically given the transition function of the channel $p(\mathbf{y}|\mathbf{x})$. Therefore, the problem of obtaining the MIR reduces to computing the entropy rate of the channel's output $H(\mathbf{Y})$. According to Shannon–McMillan–Breimann theorem [46], for a stationary and ergodic channel, the entropy rate is given by

$$-\frac{1}{n}\log p(\mathbf{y}) \to H(Y), \tag{14}$$

as $n \to \infty$ with probability 1. Therefore, to calculate the information rate, one needs to calculate the marginal output distribution $p(y)$ in the limit of large systems.

We also note that by computing the capacity of TDMR channels, we can estimate the amount of channel bits that can be reliably stored on a single grain on an average. We denote this concept by the information rate per grain and write it as D. Typically, D is considerably less than 1. Let us denote ρ as the average number of grains per nanometer square. Then, D can be computed by

$$D = \frac{\text{MIR}}{\rho \times BL \times TW} \tag{15}$$

so that the information rate provides us with another important TDMR technology metric.

D. A Trellis-Based Capacity Estimation Method

As previously described, estimating the capacity requires computing the information rate. Sections III-E and III-Fdetail two methods to perform this task.

Theforward/backwardalgorithm(alsoknownastheBCJR algorithm) [54] and the Viterbi algorithm (VA) [60], [61] are two well-known trellis-based algorithms for optimal symbol MAP detection and ML sequence detection, respectively. Indeed, both the BCJR algorithm and the VA have been shown to be equivalent to exact graphical inference in 1-D [62]. However, exact inference for 2-D channel constraints is hard [63], [64], and is increasingly difficult in the presence of strong restrictions of graphical model topology [65]. The method used to determine the achievable information rate is to estimate the MIR between the channel's input $\mathbf{X}$ and output $\mathbf{Y}$ by modeling the channel as a finite-state machine and then using the forward recursion of the BCJR algorithm [53] over the channel's trellis to compute the channel's output marginal $p(\mathbf{y})$ [32], [33]. The finite-state machine of the TDMR channel (12) can be described by the binary input alphabet $\mathcal{X}$, output alphabet $\mathcal{Y}$, finite set of states S, and by the conditional probability density function $p(y_k, s_k \,|\, s_{k-1})$ where $y_k \in \mathbf{y}$, s_k is the current state, and s_{k-1} is the previous state. The output sequence $\mathbf{y} = (y_1, y_2, \ldots, y_n)$ is a sequence of conditionally independent random variables for a given realization of the nonobservable state sequence $\mathbf{s} = (s_0, s_1, \ldots, s_n)$. The output's probability is conditioned on the state transition. We can write

$$p(y_k, s_k \,|\, s_{k-1}) = p(y_k \,|\, s_k, s_{k-1}) p(s_k \,|\, s_{k-1}), \quad k = 1, 2, \ldots. \tag{16}$$

The joint output probability distribution $p(\mathbf{y})$ is then given by

$$p(\mathbf{y}) = \sum_{\mathbf{s}} p(\mathbf{y}, \mathbf{s}) \tag{17}$$

where the summation goes over all $\mathcal{S}^{n+1}$ terms. We note that

$$p(\mathbf{y}, \mathbf{s}) = p(s_0) \prod_{k=1}^{n} p(y_k, s_k \,|\, s_{k-1}). \tag{18}$$

Therefore, we have

$$p(\mathbf{y}) = \sum_{s} p(s_0) \prod_{k=1}^{n} p(y_k, s_k \,|\, s_{k-1}). \tag{19}$$

For any given block length n and any given channel output $\mathbf{y} = (y_1, y_2, \ldots, y_n)$, the probability $p(\mathbf{y})$ can be computed using the forward recursion of the BCJR algorithm [53], which operates on the trellis of the channel. For this computation, each trellis branch b at time k is assigned the metric $\mu(b_k)$ such that

$$\mu(b_k) = p(y_k, s_k \,|\, s_{k-1}) = p(y_k \,|\, s_k, s_{k-1}) p(s_k \,|\, s_{k-1}) \tag{20}$$

where $p(s_k \,|\, s_{k-1})$ is the probability of transition from state s_{k-1} to s_k and $p(y_k \,|\, s_k, s_{k-1})$ is the distribution of noise. The trellis is then processed from left (initial states) to right (final states) computing the state metrics $\alpha(s_k)$ for $k = 1, 2, \ldots$, according to the rule

$$\alpha(s_k) = \sum_{s_{k-1}} \lambda_k \alpha(s_{k-1}) \mu(b_k) \tag{21}$$

where λ_k is a scale factor for the kth trellis section. If λ_k is chosen such that, for each time k, the sum of the time-k state metrics equals 1, then

$$\sum_{k=1}^{n} \log(\lambda_k) \to -\log(p(\mathbf{y})) \tag{22}$$

as $n \to \infty$. Then, using (14), we can estimate the MIR of TDMR channel.

E. GBP-Based Capacity Estimation Method

Probabilistic inference problems using graphical models are important in a wide variety of applications, including statistical physics, artificial intelligence, signal processing, and coding theory [66], [67]. Message passing algorithms are a class of practical methods to solve such problems. These problems can all be reformulated as the computation of marginal probabilities on factor graphs [68]. Traditional low-complexity approximate algorithms for solving these problems are based on belief propagation (BP) [69], [70] which operate on a graphical model of a channel. BP, as an algorithm to compute marginals of functions on a graphical model, has its roots in the broad class of Bayesian inference problems [71].

It is well known that the BP algorithm gives exact inference only on cycle-free graphs (trees). It has been also observed that in some applications the BP can provide close approximations to exact marginals on loopy graphs. However, an understanding of the behavior of BP in the latter case is far from complete. Moreover, it is known that BP does not perform well on graphs which contain a large number of short cycles. The problem

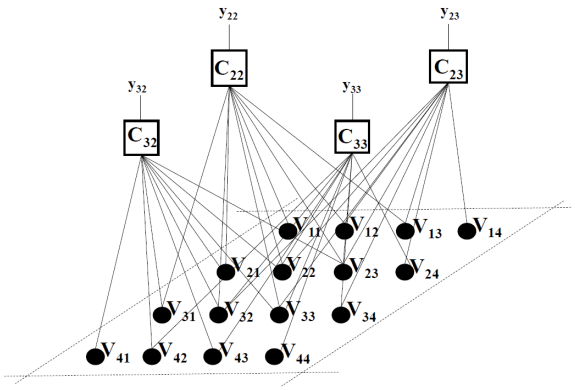


Fig. 10. *Factor graph of a 4 × 4 lattice square of random variables* $V = [V_{i,j}]_{i=1\ j=1}^{4\ \ 4}$ *where every 3 × 3 lattice square of variables is controlled by a local function* $C_{i',j'}$*. The variable nodes* $V_{i,j}$ *s are shown with circles and factor nodes* $C_{i',j'}$ *with squares where (i, j) and* (i', j') *specify the position of the node in the lattice square.*

of TDMR channel capacity estimation is considered as one of the problems corresponding to a factor graph with many short cycles. There are many cycles in a TDMR channel factor graph (see Fig. 10) which invalidates the tree-like assumption used in BP which in turn leads to poor performance of BP. A new class of message passing algorithm called GBP is introduced in [57] to solve this problem. A powerful conceptual framework for finite-dimensional lattice models is the cluster variation method by Kikuchi [72] (see [73] and [74]). In particular, we rely on the extension of the cluster variation method, called region graph method proposed by Yedidia *et al.* [57].

The major difference between GBP and BP is that GBP benefits from region-to-region message passing instead of the node-to-node message passing algorithm of BP. Consequently, GBP works well in the presence of short cycles, making it suitable for 2-D channel detection and capacity estimation problems. In practice, GBP algorithms can often dramatically outperform BP algorithms in either accuracy or convergence properties. There is a strong connection between 2-D channels and basic models in statistical mechanics. The output probabilities from a 2-D channel actually correspond to a Boltzmann distribution of an Ising Hamiltonian, with pairwise interactions and external random fields [75], [76]. The difficulty in estimating *a posteriori* probabilities lies in estimating the partition function of factor graphs, or similarly, the free energy in statistical physics. The field of statistical mechanics has devoted considerable effort to the development of methods for calculating the free energy. However, evaluating the free energy of infinitely large 2-D channels is infeasible due to the intractable computations, and one must resort to approximate methods. For the case of capacity estimation of TDMR channels, the GBP algorithm can be utilized to estimate the marginal distribution from the channel outputs and consequently the channel capacity. In the rest of the paper, we explain the method used to estimate the MIR using the GBP algorithm. Later, we apply belief propagation to efficiently decode LDPC codes applied to the TDMR read process.

We provide definitions required for using the GBP algorithm for estimating the capacity of TDMR channels. The GBP algorithm as a message passing algorithm can operate on the region graph of the TDMR channel to compute the marginal probabilities. The beliefs of each region as an output of the GBP algorithm is an approximation of the marginal probability of each region. As the GBP is a message passing algorithm, we first introduce the graphical representation for the procedure.

The factor graph is a bipartite graph representing the factorization of a function which consists of a set of random variables $\mathbf{V}$ and a set of local functions (local constraints) $\mathbf{F}$. In the factor graph, random variables $V_i \in \mathbf{V}$ are represented by circles (variable node) and local functions $f_j \in \mathbf{F}$ are demonstrated by squares (factor node). A variable node V_i is connected to a factor node f_j if and only if V_i is an argument of f_j. Fig. 10 depicts the factor graph corresponding to a 4×4 grid where each 3×3 square region is locally constrained by a factor node.

The region graph of the given graphical model is generated according to the cluster variation method [57]. In order to obtain the region graph, a parent region R is specified by a set of variable nodes and factor nodes such that if $f_j \in R$, then all the variable nodes connected to f_j must be in R. For the factor graph of 2-D-ISI constraint depicted in Fig. 10, the region graph is provided in Fig. 11. In this example, we choose each factor node to be in a separate parent region for simplicity. The variable nodes connected to the factor node also reside in that region. The child regions of a region graph are then constructed by taking the intersection of the parent regions, the intersections of the intersections, and so on.

The factor function $f(\mathbf{x}_{C_{i,j}})$ is a function of variables of $C_{i,j}$. In the case of capacity estimation, $f(\mathbf{x}_{C_{i,j}}) = p(y_{i,j} | \mathbf{x}_{C_{i,j}})$. In general, the local constraint is the same for all the parent regions.

The partition function Z and the Helmholtz free energy F_H are closely related terms in statistical physics, satisfying

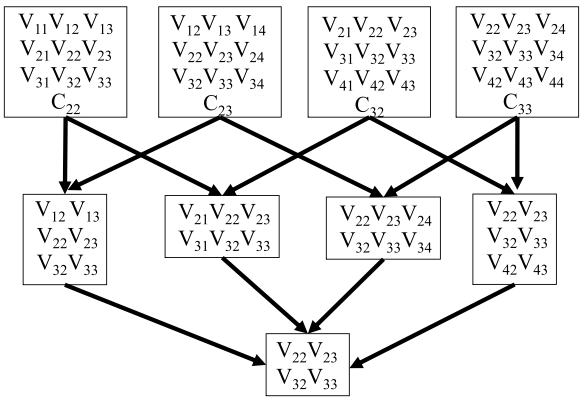


Fig. 11. *The region graph representation of the factor graph given in Fig. 10.*

$F_H = -\ln Z$. For the purpose of estimating the information rate, we define the partition function as

$$Z(\mathbf{y}) = \sum_{\mathbf{x}} \prod_{i,j} p(y_{i,j}|\mathbf{x}_{C_{i,j}}) = \sum_{\mathbf{x}} p(\mathbf{y}|\mathbf{x}) \tag{23}$$

where $f(\mathbf{x}_{C_{i,j}})$ is the factor function explained above.

As we discussed, the problem of estimating the MIR reduces to finding an estimation of the entropy of the channel output $\mathbf{y}$. For this purpose, we use the empirical averaging in the form of

$$H(\mathbf{Y}) = -\mathbf{E}_{\mathbf{y}} \log p(\mathbf{y}) \approx -\frac{1}{L}\sum_{l=1}^{L} \log p(\mathbf{y}^{(l)}) \tag{24}$$

where L is the number of samples $\mathbf{y}$ drawn according to $p(\mathbf{y})$. Applying Bayes' law and using the channel model distribution, $p(\mathbf{y})$ can be written as

$$p(\mathbf{y}^{(l)}) = \sum_{\mathbf{x}} p(\mathbf{x})\, p(\mathbf{y}^{(l)}|\mathbf{x}) \tag{25}$$

where $\sum_{\mathbf{x}}$ corresponds to a sum over all possible $\mathbf{x} \in \mathcal{X}$. The output entropy reduces to

$$\begin{aligned} H(Y) &= -\frac{1}{L}\sum_{i=1}^{L} \log\left(\frac{1}{|\mathcal{X}|} Z(y^{(l)})\right) \\ &= \log(|\mathcal{X}|) - \frac{1}{L}\sum_{i=1}^{L} \log\left(Z(y^{(l)})\right) \end{aligned} \tag{26}$$

where the input distribution is considered to be uniform, i.e., $p(\mathbf{x}) = 1/|\mathcal{X}|$. Therefore, the problem of estimating the mutual information rate of a TDMR system reduces to the problem of estimating $\sum_{\mathbf{x}} p(\mathbf{y}^{(l)}|\mathbf{x}) = Z(\mathbf{y}^{(l)})$ as in (23). The indicator function can be written as the product of local kernels, each having some subset of $\mathbf{x}$ as an argument, i.e., $f(\mathbf{x}) = \prod_a f_a(\mathbf{x}_a)$, where the indices a of the local kernels correspond, for example, to the set of all the three adjacent bits in the horizontal and vertical direction. Computing Z can be done by the finding the region-based free energy estimate. More precisely, the Helmholtz free energy F_H can be estimated using the region-based free energy approximation technique, giving the partition function Z. If the GBP is used to compute the beliefs of each region $[b_R(\mathbf{x}_R)]$, using the estimated beliefs, the estimate of free energy $\hat{F}_H$ can be computed from

$$\hat{F}_H = \sum_{R\in\mathcal{R}} c_R \sum_{\mathbf{x}_R} b_R(\mathbf{x}_R)\left(\ln\, b_R(\mathbf{x}_R) - \ln \prod_{a\in A_R} f_a(\mathbf{x}_a)\right) \tag{27}$$

where $\mathcal{R}$ is the set of all regions, c_R is the counting number, $\mathbf{x}_R$ is the set of variables in R, and A_R is the set of local kernels in region R. For formulating the GBP, we use the parent-to-child method [57]. In this method, there is only one kind of message passed between regions, and the belief of any region is the product of all the local factors in the region, multiplied by the messages coming into that region and to its descendants from outside. Each region R has a belief $b_R(\mathbf{x}_R)$ given by [57]

$$\begin{aligned} b_R(\mathbf{x}_R) &= \prod_{a\in\mathbf{A}_R} f_a(\mathbf{x}_a)\left(\prod_{P\in\mathcal{P}(R)} m_{P\to R}(\mathbf{x}_R)\right) \\ &= \left(\prod_{D\in\mathcal{D}(R)} \prod_{P'\in\mathcal{P}(D)\setminus\mathcal{E}(R)} m_{P'\to D}(\mathbf{x}_D)\right) \end{aligned} \tag{28}$$

where A_R is the set of elements in region R and the $f_a(\mathbf{x}_a)$ are the local factors of region R. $\mathcal{P}_R$ and $\mathcal{D}(R)$ are, respectively, the parent and descendant regions of R. $\mathcal{E}(R) = R \cup \mathcal{D}(R)$ and $\mathcal{P}(D)\setminus\mathcal{E}(R)$ is the set of all regions that are parents of region D except for R and descendants of R. The message-update rule in the parent-to-child algorithm is

$$m_{P\to R}(\mathbf{x}_R) = \frac{\sum \prod_{\mathbf{x}_{P\setminus R}} \prod_{a\in F_{P\setminus R}} f_a(\mathbf{x}_a) \prod_{(I,J)\in N(P,R)} m_{I\to J}(\mathbf{x}_J)}{\prod_{(I,J)\in D(P,R)} m_{I\to J}(\mathbf{x}_J)} \tag{29}$$

where the set $N(P,R)$ is the set of all connected pairs of regions (I,J) such that $J \in \mathcal{E}(P)\setminus\mathcal{E}(R)$, while $I \notin \mathcal{E}(P)$. $D(P,R)$ is the set of all connected pairs of regions (I,J) such that $J \in \mathcal{E}(R)$, while $I \in \mathcal{E}(P)\setminus\mathcal{E}(R)$. $F_{P\setminus R}$ is a set of factor nodes in the region $P\setminus R$.

F. Voronoi Channel Capacity Estimation

In this section, we intend to estimate the MIR by using the GBP algorithm for an $M \times N$ magnetic medium modeled by the Voronoi grain models. We obtain lower and upper bounds on the GBP-based MIR estimation for a Voronoi channel. The lower and upper bounds merge to the actual value for the MIR estimation of the Voronoi channel with increasing dimensions of the 2-D array. We investigate the convergence rates for different sizes of Voronoi-based magnetic medium. We explain our approaches for obtaining lower and upper bounds using the GBP algorithm.

- Lower bound: No information about the boundaries of the magnetic medium is provided to the GBP MIR estimator. In order to compute the beliefs of the boundary regions, we assume that all the states of the boundary regions are equiprobable. Under this assumption and using the GBP algorithm as described before, we establish a lower bound on the MIR of a TDMR system.
- Upper bound: The boundary information of the medium is known to the MIR estimator. For boundary regions, the values of the boundary variable nodes are given and treated as deterministic in the GBP algorithm. For this case, we compute an upper bound on the MIR of the Voronoi channel.

Fig. 12 shows lower and upper bounds on the estimation of MIR for the Voronoi channel with random 20×20 and 40×40 bit arrays generated according to the uniform distribution. In fact, MIR is estimated for uniform input distribution; this can also be interpreted as the symmetric information rate. The parameters of the TDMR_1 system simulated are given in Table 1. Fig. 12 demonstrates the convergence of the estimated MIR lower and upper bound when the array dimensions increases. It is worth noting that the convergence rate of the upper bound is

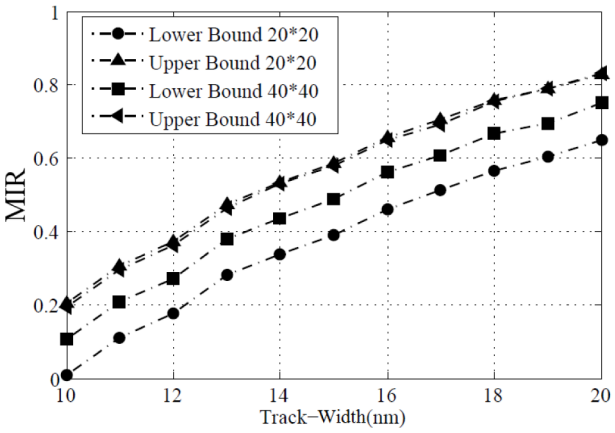


Fig. 12. *Lower and upper bounds on the MIR of the $TDMR_1$ system with the Voronoi channel model. It is shown that increasing the track width decreases media noise leading to the MIR increment.*

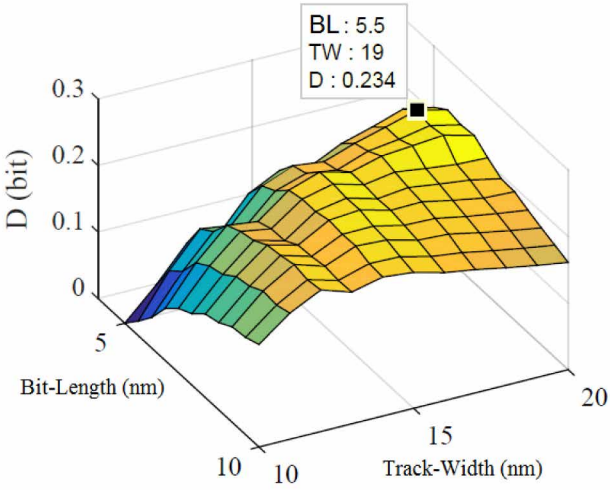


Fig. 13. *Finding the optimal TW and BL by maximizing information rate per grain D for the $TDMR_2$ system with the parameters provided in Table 1. The MIR for maximum D is found to be empirically approximately 0.6 under these conditions.*

much faster than the lower bound. In other words, having an infinite array provides sufficient information such that the boundary bits can be considered to be known in the MIR estimation for a large enough, but finite case, like a 40 × 40 array.

G. Voronoi Channel BAR Optimization

The bit error rate after detection is a useful performance metric when optimizing the multireader geometry for a given TW and BL, but it cannot be used to optimize the TW and BL parameters themselves. Here we use the MIR between the input sequence of written bits on the magnetic medium (in this case Voronoi channel) and the output sequence as a more comprehensive metric that can be used to simultaneously optimize all the relevant parameters. Suppose that in the TDMR system, the reader and the medium parameters are fixed. Therefore, in order to achieve the highest achievable areal density, we have to optimize TW and BL by maximizing D. Fig. 13 shows the optimal TW and BL which are obtained by maximizing the bit per grain for the $TDMR_2$ system with the parameters given in Table 1. The number of bit cells in the cross-track and down-track direction is 20 × 20. We are now ready to tackle the main innovations required for realizing TDMR systems. Sections IV and V discuss signal processing for TDMR; afterwards, we consider error-correcting codes suitable for TDMR.

Table 1 All the Parameters in the Table Are in Nanometers. We Denote $n_1:n_2:n_3 = \{n_1, n_1+n_2, n_1+2n_2, \ldots, n_3\}$. CTC= 10 nm

	TW	BL	$PW50_x$	$PW50_y$
$TDMR_1$	10:1:20	7	20	14
$TDMR_2$	10:1:20	5:0.5:10	20	10

IV. SIGNAL PROCESSING FOR SHINGLED SYSTEMS

This section focuses on signal processing techniques for TDMR based on shingling. We start with single-track and multitrack detection in this section and continue with timing recovery in Section V.

One of the tools available to TDMR systems is the presence of multiple read heads. Multiple readers can be leveraged by the read channel in two ways. In single-track detection, the readers are positioned over a single track of interest to improve the reliability of the recovered bits. In multitrack detection, on the other hand, the readers are positioned over two tracks, with the aim of recovering the bits from both the tracks simultaneously. In the following, we describe signal processing strategies for these two different scenarios.

A. Single-Track Detection

First-generation implementations of TDMR use multiple readers to recover the bits from only a single track of interest [77]–[79], a scenario known as single-track detection. Extending the partial response strategy from the single-reader case to the multiple-reader case leads to the read channel architecture shown in Fig. 14. Here, each read-back waveform is separately equalized before being added together, which is equivalent to applying the read-back waveforms to a multiple-input–single-output (MISO) equalizer. As in the single-reader case, the equalizer coefficients are typically chosen jointly with the target coefficients according to an minimum mean square error (MMSE) criterion, so as to minimize the mean square error (MSE) between the equalizer output and the response of the bits of the desired track to the target impulse response.

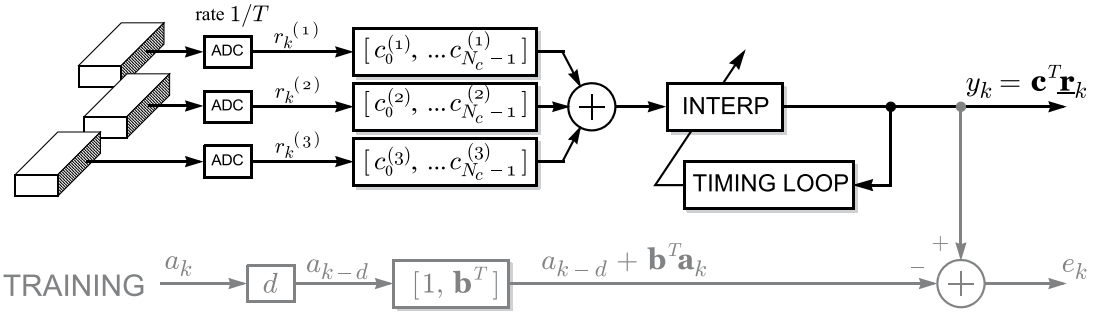


Fig. 14. ***Signal processing architecture for single-track detection with multiple readers.***

In the process, the equalizer suppresses both ITI from interfering tracks as well as ISI beyond the extent of the target length, both of which serve to reduce the number of states and hence the complexity of the trellis-based detector that follows. Because the equalizer suppresses the ITI, the detector that follows can be a traditional 1-D trellis-based detector, such as a soft-output Viterbi detector or a BCJR detector, with pattern-dependent noise prediction.

1) Single-Track Target and Equalizer Optimization: The equalizer and target can be jointly optimized by extending the principles of generalized partial response [80] to the multiple-reader setting [81]. As illustrated in Fig. 14 for the case of $N = 3$ readers, the ith read-back signal is fed to an equalizer having N_c coefficients. Let $\mathbf{r}_k = [\, r_k^{(1)}, \ldots, r_k^{(N)} \,]^T$ denote the $N \times 1$ vector of N read-back waveform samples at time k, where $r_k^{(i)}$ denotes the kth sample from the ith reader for $i \in 1, \ldots, N$. For now we assume that the analog-to-digital converter (ADC) sampling rate is synchronous with the bit rate, so that no timing recovery is necessary, and so that the interpolation filter after the equalizer is the identity. (Timing recovery will be considered in Section V.) Similarly, let $\mathbf{c}_k = [\, c_k^{(1)}, \ldots, c_k^{(N)} \,]^T$ denote the kth $N \times 1$ vector-valued MISO equalizer coefficient, where $c_k^{(i)}$ denotes the kth coefficient ($k \in \{0, \ldots, N_c - 1\}$) of the ith equalizer. The equalizer output can then be written as $y_k = \mathbf{c}^T \underline{\mathbf{r}}_k$, where $\mathbf{c} = [\, \mathbf{c}_0^T, \ldots, \mathbf{c}_{N_c-1}^T \,]^T$ of dimension $(NN_c) \times 1$ represents the entire MISO equalizer and $\underline{\mathbf{r}}_k = [\, \mathbf{r}_k^T, \ldots, \mathbf{r}_{k-N_c+1}^T \,]^T$, with dimension $(NN_c) \times 1$. The target is constrained to be monic, of the form $[\, 1, \mathbf{b}^T \,]$, where $\mathbf{b} = [\, b_1, \ldots, b_\mu \,]^T$ is the target tail and μ is the target memory. Filtering the information symbols by the desired target yields the signal $a_{k-d} + \mathbf{b}^T \mathbf{a}_k$, where d is the equalizer delay parameter, and where $\mathbf{a}_k = [\, a_{k-d-1}, \ldots, a_{k-d-\mu} \,]^T$. In these terms, the optimization problem is to jointly choose the equalizer $\mathbf{c}$ and target tail $\mathbf{b}$ to minimize the MSE $\mathbf{E}[\, e_k^2 \,]$, where $e_k = \mathbf{c}^T \underline{\mathbf{r}}_k - a_{k-d} - \mathbf{b}^T \mathbf{a}_k = \mathbf{w}^T \mathbf{v}_k - a_{k-d}$, where we have combined the equalizer and target unknowns into the single vector $\mathbf{w} = [\, \mathbf{c}^T, -\mathbf{b}^T \,]^T$, and where $\mathbf{v}_k = [\, \underline{\mathbf{r}}_k^T, \mathbf{a}_k^T \,]^T$. Here, $\mathbf{v}_k$ and $\mathbf{w}$ are of dimensions $(NN_c + \mu) \times 1$. The MSE is quadratic in $\mathbf{w}$, with the equalizer and target that jointly minimize MSE given by

$$\mathrm{w} = \mathbf{R}_{\mathbf{vv}}^{-1} \mathrm{p} \tag{30}$$

where $\mathbf{R}_{\mathbf{vv}} = \mathbf{E}[\, \mathbf{v}_k \mathbf{v}_k^T \,]$ and $\mathbf{p} = \mathbf{E}[\, \mathbf{v}_k a_{k-d} \,]$.

2) Synchronization for Single-Track Detectors: While multiple readers per slider are beginning to see deployment, most practical designs will still have only a single write head. Therefore, the bits on neighboring tracks will be asynchronous with each other, with variations in disk rotational speeds leading to neighboring tracks to have not only different bit phases, but also having slightly different bit rates (frequency offset).

A fundamental question arises: Must we have knowledge of the timing offsets for the bits of an interfering track when mitigating its interference? Here, we demonstrate that the answer is no for the special case of linear ITI suppression and constant timing phase offsets; in this case, the ITI can be suppressed asynchronously (without any knowledge of its timing phase), so that a synchronization loop is needed only for the track or tracks of interest. A clear benefit is that synchronization is not needed for each ADC (or equivalently each read head); rather it is only needed for each detected track, and it can leverage existing and mature 1-D synchronization strategies.

We begin by describing an efficient model for asynchronous tracks. Let T denote the ADC sampling period, and let $T + \Delta T$ denote the bit period of an asynchronous signal. Consider the diagram in Fig. 15(a), which shows a continuous-time signal $s(t) = \sum_k a_k h(t - k(T + \Delta T))$ with bit period $T + \Delta T$ being sampled asynchronously by an ADC with sampling period T, where $a_k \in \{\pm 1\}$ is the bit sequence, and where the pulse shape is $h(t) = \sum_k h_k g(t - k(T + \Delta T))$,

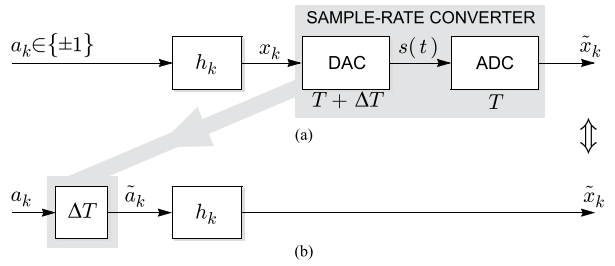


Fig. 15. ***Modeling frequency offset.***

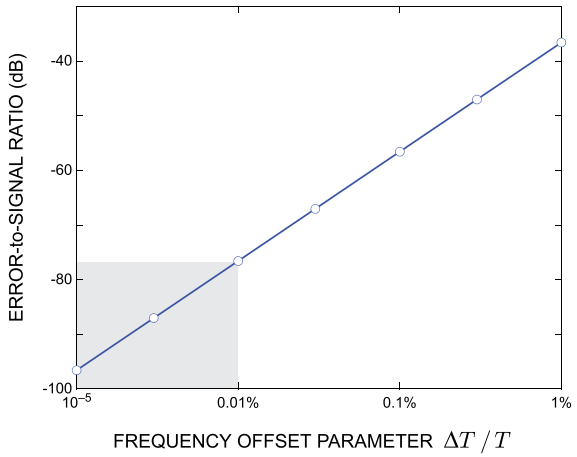


Fig. 16. ***The modeling error is small for reasonable frequency offsets.***

where $g(t) = \sin(\pi t/(T+\Delta T))/(\pi t/(T+\Delta T))$ is the minimum-bandwidth pulse shape for the bit rate $1/(T+\Delta T)$. The back-to-back cascade of the digital-to-analog converter (DAC) and ADC is a sample-rate converter, which can be interchanged with the discrete-time filter h_k with good accuracy when the frequency offset parameter ΔT is small. This leads to the fully digital model shown in Fig. 15(b), where the binary bits $a_k \in \{\pm 1\}$ are first applied to the sample-rate converter, producing a "delayed" version $\tilde{a}_k \in \mathbb{R}$ of the bits, where $\tilde{a}_k = \sum_i a_i \mathrm{sinc}(k - i - k\Delta T/T)$; these delayed bits are then applied to the same digital filter h_k that the original bits would have seen, had the ADC been synchronized. As illustrated in Fig. 16, the modeling error is more than 70 dB below the signal level and well below the noise floor for reasonable conditions, when the frequency offset parameter is $\Delta T/T < 10^{-4}$.

What makes the equivalent model in Fig. 16(b) so powerful is the unexpected result that the mean and autocorrelation function for the delayed bits $\tilde{a}_k$ are identical to those of the original bits a_k, namely $\mathbf{E}[\tilde{a}_k] = 0$ and $\mathbf{E}[\tilde{a}_k \tilde{a}_{k+m}] = \delta_m$ [82]. In other words, the value of the timing offsets has no impact on the second-order statistics. If synchronous tracks leads to the linear model $\mathbf{r}_k = \sum_i \mathbf{H}_{k-i} \mathrm{a}_i + \mathbf{n}_k$ for the kth vector of ADC samples, then the impact of asynchrony can be accurately modeled by replacing the bits by their delayed versions according to $\mathbf{r}_k = \sum_i \mathbf{H}_{k-i} \mathbf{a}_i + \mathbf{n}_k$. In principle, this means that, if we knew the training bits and timing offsets and thus knew the $\{\tilde{a}_k^{(i)}\}$, we could design our equalizer and target according to (30) but with the delayed bits as our reference [with $\tilde{a}_k^{(0)}$ in place of a_k in the definitions of $\mathbf{v}_k$ and $\mathbf{p}$]. We thus arrive at the key result that the equalizer and target coefficients are transparent to any timing offsets. As a result, ITI can be suppressed asynchronously, before synchronization. A practical implication of this result is that we do not need a separate synchronization loop for each reader; the equalizer coefficients will be invariant to the timing offsets of the interfering tracks. Instead, a single 1-D timing loop is sufficient after the equalizer and before the detector, as shown in Fig. 14.

B. Multitrack Detection

Compared to the single-track detection architecture of the previous section, significant areal density gains can be expected when the multiple readers are used to jointly detect two or more tracks, a scenario known as multitrack detection [83]–[85]. The move from single-track detection to multitrack detection is conceptually similar to the move in the early 1990s from peak detection to sequence detection; from the perspective of a peak detector, ISI is an impediment to be avoided, while from the perspective of a sequence detector, ISI contains valuable signal energy that can be exploited to improve performance. Similarly, single-track detectors avoid ITI, while multitrack detectors can embrace it. Furthermore, multitrack detectors open up the possibility of exploiting error-control coding and modulation coding across tracks, as well as the possibility of cross-track pattern-dependent noise prediction. The concept of using multiple readers to jointly detect multiple tracks dates back over two decades [83], [84], but it has only been recently considered for practical implementation. In a recent work on multihead multitrack detection [86], [87], the authors propose a detector that uses a different trellis structure whose output labels are independent of the intertrack interference (ITI) level, with ITI dependence appearing only in a scale factor for suitably weighing the computed path metrics in order to retain ML optimality. The detector formulation facilitates the design of a gain loop structure that can track the time-varying ITI and provide ITI estimates to adaptively adjust the weights in the path metric evaluation. The authors evaluate the efficacy of the detector through theory and simulations. Let us begin with a treatment on multitrack target and equalizer design.

1) Multitrack Target and Equalizer Optimization: As illustrated in Fig. 17 for the case of $N = 3$ readers and two tracks to be detected jointly, the N read-back sampled waveforms are fed to an N-in–2-out MIMO equalizer. Post multitrack equalization and detection, we will discuss synchronization for multitrack detection; here we assume that the tracks being detected are synchronous with both each other and the ADC sampling rate, so that the interpolation filters in the figure are identity operators, resulting in $\tilde{\mathbf{a}}_k = \mathbf{a}_k$. The 2×1 vector-valued equalizer output can be written compactly as $\mathbf{y}_k = \mathbf{C}^T \underline{\mathbf{r}}_k$, where $\underline{\mathbf{r}}_k$ was defined previously, and where $\mathbf{C} = [\mathbf{C}_0^T, \ldots, \mathbf{C}_{N_c-1}^T]^T$ represents the MIMO equalizer, where each $\mathbf{C}_k$ is a $2 \times N$ matrix-valued coefficient. The target in this case is a two-in–two-output MIMO filter with transfer function

$$\mathbf{G}(D) = \sum_{k=0}^{\mu} \mathbf{G}_k D^k \tag{31}$$

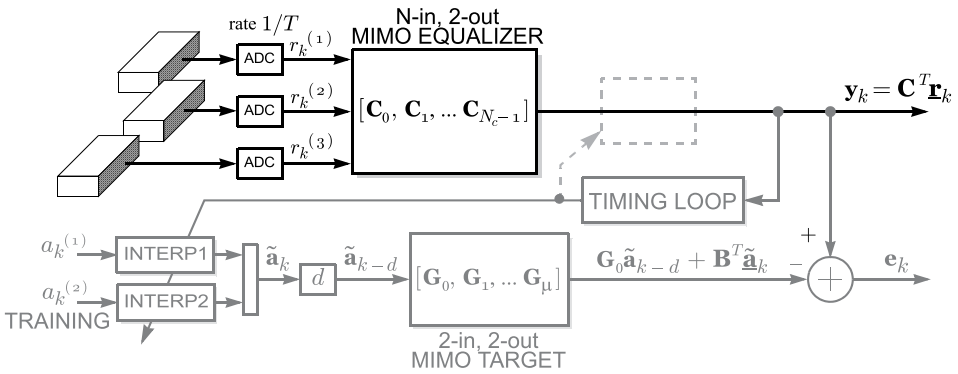


Fig. 17. ***Signal processing architecture for multitrack detection with multiple readers.***

where μ is the target memory parameter.

Generalizing the monic constraint in the single-track case to the MIMO case, let us impose the constraint that the zeroth coefficient of the target is lower triangular with ones on the diagonal [88], i.e.,

$$\mathbf{G}_0 = \begin{bmatrix} 1 & 0 \\ G_{2,1}^{(0)} & 1 \end{bmatrix}. \tag{32}$$

Rather than viewing the target as a single matrix-valued filter, we can equivalently view it is a set of four scalar-valued target filters, where the ith row and jth column $G_{ij}(D)$ of $\mathbf{G}(D)$ represent the scalar target from the jth track of interest to the ith equalizer output ($i, j \in \{1, 2\}$). In terms of these scalar targets, the monic constraint of (32) implies that both $G_{11}(D)$ and $G_{22}(D)$ are monic in the scalar sense, and further that $G_{12}(D)$ is strictly causal. Filtering the information symbols by the desired target yields the signal $\mathbf{G}_0\mathbf{a}_{k-d} + \mathbf{B}^T\underline{\mathbf{a}}_k$, where again d is the equalizer delay parameter, and where we have introduced the target "tail" $\mathbf{B} = [\mathbf{G}_1, \ldots, \mathbf{G}_\mu]^T$. In these terms, the 2×1 equalizer error vector at time k can be written as

$$\mathbf{e}_k = \mathbf{C}^T\underline{\mathbf{r}}_k - \mathbf{G}_0\mathbf{a}_{kd} - \mathbf{B}^T\underline{\mathbf{a}}_k. \tag{33}$$

The MMSE optimization problem is to jointly choose the equalizer $\mathbf{C}$ and target $(G_{2,1}^{(0)}, \mathbf{B})$ to minimize the MSE $\mathbf{E}[\,\|\mathbf{e}\|^2]$. The error can be simplified by cascading the equalizer coefficients and target tail into a single matrix $\mathbf{W} = [\mathbf{C}^T, -\mathbf{B}^T]^T$, so that the error becomes

$$\mathbf{e}_k = \mathbf{W}^T\mathbf{v}_k - \mathbf{G}_0\mathbf{a}_{k-d}. \tag{34}$$

The MSE is quadratic in $\mathbf{W}$, as becomes evident by completing the square and writing the MSE as

$$\begin{aligned} \text{MSE} &= \text{tr}\{\mathbf{e}_k\mathbf{e}_k^T\} \\ &= \text{tr}\{E((\mathbf{W}^T\mathbf{v}_k - \mathbf{G}_0\mathbf{a}_{k-d})(\mathbf{W}^T\mathbf{v}_k - \mathbf{G}_0\mathbf{a}_{k-d})^T)\} \\ &= \text{tr}\{(\mathbf{W} - \mathbf{R}_{\mathbf{vv}}^{-1}\mathbf{R}_{\mathbf{va}}\mathbf{G}_0^T)^T\mathbf{R}_{\mathbf{vv}}(\mathbf{W} - \mathbf{R}_{\mathbf{vv}}^{-1}\mathbf{R}_{\mathbf{va}}\mathbf{G}_0^T) \\ &\quad + \mathbf{G}_0\mathbf{G}_0^T - \mathbf{G}_0\mathbf{R}_{\mathbf{va}}^T\mathbf{R}_{\mathbf{vv}}\mathbf{R}_{\mathbf{va}}\mathbf{G}_0^T\} \end{aligned} \tag{35}$$

where $\mathbf{R}_{\mathbf{vv}} = \mathbf{E}[\mathbf{v}_k\mathbf{v}_k^T]$ and $\mathbf{R}_{\mathbf{va}} = \mathbf{E}[\mathbf{v}_k\mathbf{a}_{k-d}^T]$. Whatever choice is made for $\mathbf{G}_0$, the optimal $\mathbf{W}$ will make the quadratic form in the trace zero by taking

$$\mathbf{W} = \mathbf{R}_{\mathbf{vv}}^{-1}\mathbf{R}_{\mathbf{va}}\mathbf{G}_0^T. \tag{36}$$

We choose $\mathbf{G}_0$ to minimize the MSE that results from this choice, namely to minimize

$$\begin{aligned} \text{MSE} &= \text{tr}\{\mathbf{G}_0(\mathbf{I} - \mathbf{R}_{\mathbf{va}}^T\mathbf{R}_{\mathbf{vv}}^{-1}\mathbf{R}_{\mathbf{va}})\mathbf{G}_0^T\} \\ &= \text{tr}\{\mathbf{G}_0\mathbf{M}\mathbf{D}^2\mathbf{M}^T\mathbf{G}_0^T\} \end{aligned} \tag{37}$$

where we have introduced the Cholesky decomposition $\mathbf{I} - \mathbf{R}_{\mathbf{va}}^T\mathbf{R}_{\mathbf{vv}}^{-1}\mathbf{R}_{\mathbf{va}} = \mathbf{M}\mathbf{D}^2\mathbf{M}^T$, where $\mathbf{L} = \mathbf{M}\mathbf{D}$ is lower triangular with nonnegative diagonal components, and where $\mathbf{D} = \text{diag}\{\mathbf{L}\}$ is a diagonal matrix containing only the diagonal components of $\mathbf{L}$, so that $\mathbf{M} = \mathbf{L}\mathbf{D}^{-1}$ is "monic": lower triangular with ones on the diagonal. The product $\mathbf{G}_0\mathbf{M}$ of two such monic matrices is also monic. To minimize MSE, we can do no better than to make this product the identity by choosing $\mathbf{G}_0 = \mathbf{M}^{-1}$, so that the MSE reduces to

$$\text{MSE} = \text{tr}\{\mathbf{D}^2\}. \tag{38}$$

To summarize, the MMSE solution for the equalizer $\mathbf{C}$ and monic target $(G_{2,1}^{(0)}, \mathbf{B})$ is $[\mathbf{C}^T, -\mathbf{B}^T] = \mathbf{M}^{-1}\mathbf{R}_{\mathbf{va}}^T\mathbf{R}_{\mathbf{vv}}^{-1}$ and $\mathbf{G}_0 = \mathbf{M}^{-1}$, where $\mathbf{R}_{\mathbf{vv}} = \mathbf{E}[\mathbf{v}_k\mathbf{v}_k^T]$, $\mathbf{R}_{\mathbf{va}} = \mathbf{E}[\mathbf{v}_k\mathbf{a}_{k-d}^T]$, and $\mathbf{M}$ is the monic factor in the Choleskey decomposition

$$\mathbf{I} - \mathbf{R}_{\mathbf{va}}^T\mathbf{R}_{\mathbf{vv}}^{-1}\mathbf{R}_{\mathbf{va}} = \mathbf{M}\mathbf{D}^2\mathbf{M}^T. \tag{39}$$

2) Synchronization for Multitrack Detectors: We have already seen that the synchronization problem in the single-track setting is straightforward, since off-the-shelf 1-D strategies based on a phase-locked loop (PLL) [89] or interpolative timing recovery (ITR; as shown in Fig. 14) can be applied after the MISO equalizer front end. A key attribute there was the modular nature of the system: the functions of synchronization and detection are implemented separately. The problem of detection in the face of asynchronous tracks changes drastically as we move from

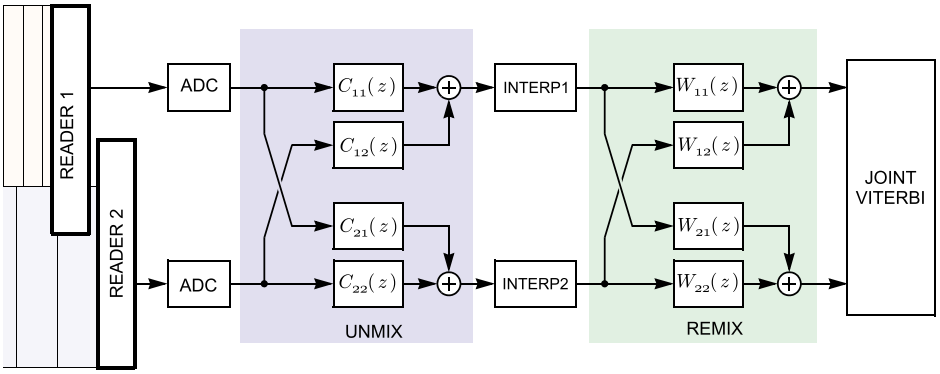


Fig. 18. ***The remix architecture for joint multitrack detection of asynchronous tracks has four stages: 1) an unmix stage, in which the contributions from the two tracks being detected are separated into two outputs by a MIMO equalizer; 2) a pair of ITR loops operating independently on the two equalizer outputs, which aim to synchronize the two tracks being detected; 3) a remix stage consisting of a MIMO filter; and 4) a joint multitrack Viterbi detector for detecting the now-synchronous tracks.***

single-track to multitrack detection. In fact, in this multitrack case, we must abandon the notion of a modular solution altogether, because it no longer makes sense to talk about synchronizing the ADC samples to two (or more) signals that are themselves asynchronous. The core issue is the impossibility of being synchronous to both tracks simultaneously: being synchronous to one necessarily implies being asynchronous to the other. The implication is that synchronization and detection can no longer be performed separately in a modular way, but instead must be performed jointly.

In the remainder of this section, we summarize the two known solutions for multitrack detection of asynchronous tracks: the remix strategy, and the rotating target strategy.

The remix strategy: The remix architecture for jointly detecting multiple asynchronous tracks is shown in Fig. 18. The proposed architecture consists of four stages, as illustrated in the figure.

- Unmix—The goal of the "unmix" stage, as its name implies, is to unmix the contributions from the two tracks of interest using a pair of MISO equalizers, so that only the first track contributes to the output of the first MISO equalizer, and only the second track contributes to the output of the second MISO equalizer. This pair of MISO equalizers can be viewed equivalently as a MIMO equalizer $\mathbf{C}(z)$ whose role is to diagonalize the cascade of the MIMO channel and the equalizer.
- Synchronize—After the unmixing stage, the two sample streams are separately synchronized using a pair of independent 1-D ITR loops, for example, based on a PLL.
- Remix—The third "remix" stage restores the nondiagonal nature of the MIMO channel by applying the MIMO filter $\mathbf{W}(z)$, which aims to recover any SNR penalty that was incurred by the unmixing stage. Any noise enhancement induced by the unmixing filter can be alleviated by the remixing filter. One promising strategy for implementing the remix stage is to make $\mathbf{W}(z)$ a MIMO whitening filter that uses a combination of temporal and spatial linear prediction [88], which would result in the spatially and temporally white noise that is beneficial for subsequent optimal detection.
- After the remix stage, the overall target seen by the (now synchronized) bits is approximately $\mathbf{W}(z)\begin{bmatrix} G_1(z) & 0 \\ 0 & G_2(z) \end{bmatrix}$, where $G_i(z)$ is the target for the ith MISO equalizer. The final step is to implement a joint (multitrack) Viterbi detector for the two tracks of interest based on this overall MIMO target.

It is useful to compare the architecture in Fig. 18 to a pair of single-track detectors operating separately on the two read-back waveforms, one aimed at recovering the bits from track 1, the other aimed at recovering the bits from track 2. Replicating the single-track detector of Fig. 14 twice leads immediately to the first two stages of Fig. 18. Thus, the only novelty in the remix architecture of Fig. 18 is in the last two stages; rather than applying the two interpolation filter outputs to different detectors, one for each track, they are detected jointly. Furthermore, the remix strategy changes the target for the joint Viterbi detector from the highly restrictive form $\begin{bmatrix} G_1(z) & 0 \\ 0 & G_2(z) \end{bmatrix}$ to the more relaxed form $\mathbf{W}(z)\begin{bmatrix} G_1(z) & 0 \\ 0 & G_2(z) \end{bmatrix}$, the latter offering better performance when chosen properly. Indeed, consider the special case where both tracks are synchronous, and hence both of the interpolation filters are identity operators. In this case, the cascade of the unmix filter and the remix filter together can realize the optimal equalizer.

The rotating target strategy: Here we describe the rotating-target (ROTAR) algorithm as a solution to the problem of jointly detecting multiple asynchronous tracks from multiple read-back waveforms [82]. The ROTAR algorithm modifies a joint Viterbi detector to have a time-varying target that accounts for the asynchrony of the tracks being detected. Per-survivor processing (PSP) is used within the Viterbi detector to estimate the timing offsets of the tracks of interest, a generalization of the 1-D per-survivor timing recovery strategy developed for single-track detection [90].

The multitrack detection architecture of Fig. 17 was originally introduced under the assumption that the two tracks being detected were synchronous; here we examine how the architecture can be generalized to handle the asynchronous case. The dashed box in the figure is there to emphasize what is not possible: the two equalizer outputs cannot be simultaneously synchronized to both tracks when the tracks themselves are asynchronous. We need a different solution.

Consider first the synchronous case: If all tracks were synchronized to the ADC sampling rate, the equalizer output would be a noisy version of feeding the bits from the tracks being detected to the MIMO target, namely

$$\mathbf{y}_k = \sum_i \mathbf{G}_i \mathbf{a}_{k-i} + \mathbf{n}_k \tag{40}$$

where $\{\mathbf{G}_0, \ldots, \mathbf{G}_\mu\}$ is the MIMO target (see Fig. 17). Adopting the efficient model for timing offsets developed earlier, the impact of having asynchronous tracks that are further asynchronous with the ADC is to simply replace the original bits $\mathbf{a}_k$ by their delayed versions $\tilde{\mathbf{a}}_k$, leading to the following model for the MIMO equalizer output in Fig. 17

$$\mathbf{y}_k = \sum_i \mathbf{G}_i \tilde{\mathbf{a}}_{k-i} + \mathbf{n}_k . \tag{41}$$

The lower half of Fig. 17 explicitly shows this model for the equalizer output, where the training bits are first fractionally delayed by a pair of time-varying interpolation filters, producing $\tilde{\mathbf{a}}_k$, and then applied to the MIMO target $\mathbf{G}(D)$. We can thus formulate a minimum-distance multitrack detector that jointly chooses the bits $\{\mathbf{a}_k\}$ to minimize the Euclidean cost

$$\sum_k \left\| \mathbf{y}_k - \sum_i \mathbf{G}_i \tilde{\mathbf{a}}_{k-i} \right\|^2 . \tag{42}$$

Rather than applying the time-varying interpolation filters to the bits, however, we choose instead to view the cascade of the interpolation filters and the fixed MIMO target $\mathbf{G}(D)$ as a time-varying target. This leads to the following equivalent cost:

$$\sum_k \left\| \mathbf{y}_k - \sum_i \widetilde{\mathbf{G}}_i(k) \mathbf{a}_{k-i} \right\|^2 \tag{43}$$

where $\{\widetilde{\mathbf{G}}_0(k), \ldots, \widetilde{\mathbf{G}}_\mu(k)\}$ is the MIMO target at time k.

While the time-varying target of (43) is conceptually straightforward, it is not conducive to a direct implementation. To understand why, consider an example where both tracks are synchronous with a fixed target $[\mathbf{G}_0, \mathbf{G}_1, \mathbf{0}, \mathbf{0}, \mathbf{0}, \ldots]$ having memory $\mu = 1$, and where the ADC sampling rate is larger than the bit rates by 1%. The ADC frequency offset will cause the target to drift in time; after 100 bits, the time-varying target will shift to $[\mathbf{0}, \mathbf{G}_0, \mathbf{G}_1, \mathbf{0}, \mathbf{0}, \ldots]$, with memory $\mu = 2$, and after 200 bits, it will be shift to $[\mathbf{0}, \mathbf{0}, \mathbf{G}_0, \mathbf{G}_1, \mathbf{0}, \ldots]$, with memory $\mu = 3$. The time-varying target thus has memory that grows linearly with time, which makes a Viterbi detector impractical for long sector lengths and nonnegligible frequency offsets.

The key to the ROTAR algorithm is that it tracks only the significant coefficients in the time-varying target, so that the target memory (and thus the number of states in the trellis detector) can be held constant, independent of both the sector length and the severity of the frequency offset [82]. This efficient implementation of ROTAR is based on a decomposition of the timing offsets into their integer and fractional parts, and applying the integer parts to the bits themselves $\{a_k^{(i)}\}$, so that only the fractional parts of the timing offsets are applied to the target. The resulting target is still time varying, but its memory need not grow with time, as in the above example, but instead the memory is fixed at a small value that need not be much greater than the memory of the underlying fixed target. The complexity of ROTAR can be further decreased by locking all of the ADCs to one of the tracks being detected; this reduces the memory needed for that track, leaving only the target for the asynchronous track to rotate. Simulation studies have shown that a 16-state ROTAR detector in the face of frequency offset offers the same performance as a four-state multitrack detector in the ideal case when the tracks are synchronous to each other and to the ADC sampling rate [91].

The treatment of signal processing for shingled recording is based on the "MIMO" framework for detecting bits from a handful of tracks from tens of thousands of samples received from a handful of readers. However, true 2-D detection will need a signal processing framework for detecting an array of bits from an array of asynchronous samples. This treatment will follow in Section V starting with 2-D timing recovery based on PLLs, and advancing the techniques towards a true 2-D joint timing recovery and detection scheme.

V. SIGNAL PROCESSING FOR NATIVE 2-D TIMING AND DETECTION

We begin this section starting with a discussion of the timing recovery problem when an array of asynchronous samples are received in the read-back process. The received samples suffer from timing errors, 2-D ISI and noise that are inherently 2-D. We need techniques for detecting an array of bits by overcoming all these artifacts. We first begin with the 2-D timing recovery process.

Two-dimensional timing errors can occur due to imprecisions in the servo mechanisms while reading,

as well as mechanical vibrations and shocks on the read heads at nanoscales. Within a linear approximation, the read-back signal can be modeled as a convolution of the written data and the 2-D channel impulse response with timing offsets as [92]

$$r(\boldsymbol{t}) = \sum_{\boldsymbol{k}\in\mathbb{Z}^2} d_{\boldsymbol{m}} h(\boldsymbol{t} - \boldsymbol{k}^T \boldsymbol{T} - \boldsymbol{\tau}(\boldsymbol{k})) + n(\boldsymbol{t}) \tag{44}$$

where $\boldsymbol{t} = [x, y]^T$, $\boldsymbol{k} = [m, n]^T$, $\boldsymbol{T} = \text{diag}(T_x, T_y)$, and $\boldsymbol{\tau} = [\tau_x, \tau_y]^T$. The terms T_x and T_y represent the baud rates along the x- and y-directions. Similarly, τ_x and τ_y represent the timing errors along the x- and y-directions. Binary non-return-to-zero (NRZ) data stored on the media are represented by $d_{\boldsymbol{m}}$, where $\boldsymbol{m} \in \mathbb{Z}^2$. The term $n(\boldsymbol{t})$ represents the electronic noise associated with the read-back process and can be assumed to be normally distributed in 2-D. As discussed earlier, any noise coloration due to filtering or jitter can always be whitened toward the form given by (44) using techniques described in [27].

Timing errors in TDMR can be a combination of both phase and frequency errors on a 2-D surface. Let the phase errors along the x- and y-directions be a_x and a_y, respectively. Similarly, let $\delta T_x^{(x)}$ and $\delta T_y^{(y)}$ be the frequency offsets along the x- and y-directions. The overall timing error for separable frequency offsets due to a direction dependent timing error can be modeled as

$$\boldsymbol{\tau}(\boldsymbol{k}) = \boldsymbol{A} + \boldsymbol{m}^T \boldsymbol{B} + n(\boldsymbol{k}) \tag{45}$$

where $\boldsymbol{A} = [a_x, a_y]^T$ and $\boldsymbol{B} = \text{diag}(\delta T_x^{(x)}, \delta T_y^{(y)})$.

Frequency drifts in 2-D can result in nonseparable timing offsets. These artifacts are modeled by modifying $\boldsymbol{B}$ to allow projections of the timing errors in the x- and y-directions as

$$\boldsymbol{B} = \begin{bmatrix} \delta T_x^{(x)} & \delta T_y^{(x)} \\ \delta T_x^{(y)} & \delta T_y^{(y)} \end{bmatrix} \tag{46}$$

where $\delta T_x^{(y)}$ and $\delta T_y^{(x)}$ represent the projections on the y- and x-directions due to frequency offsets. In addition, it is to be noted that modeling $\boldsymbol{B}$ as a nondiagonal matrix destroys the separability of the channel model in the read-back signal. This would invalidate any separable 2-D equalization/detection schemes in the system post or prior to the timing scheme. Nonseparable errors can occur due to both direction- and position-dependent physical errors in the servo system. We discuss several timing recovery schemes toward a full blown version of the TDMR system.

Upon sampling the read-back signal with timing errors, using the baud-rate matrix $\boldsymbol{T}$, we obtain

$$r(\boldsymbol{i}^T \boldsymbol{T}) = d_{\boldsymbol{i}} h(-\boldsymbol{\tau}(\boldsymbol{i})) + \sum_{\boldsymbol{k}\in\mathbb{Z}^2} d_{\boldsymbol{k}} h(\boldsymbol{i}\boldsymbol{T} - \boldsymbol{k}^T \boldsymbol{T} - \boldsymbol{\tau}(\boldsymbol{k})) + n(\boldsymbol{i}^T \boldsymbol{T}) \tag{47}$$

where $\boldsymbol{i} = [m, n]^T$ represents the 2-D coordinates of the samples. The first term in (47) represents the encoded bits written on the medium, evidently distorted by the presence of timing errors. The second term represents the 2-D ISI that needs to be mitigated by the equalizer. The third term is the electronic noise component, typically modeled using a 2-D Gaussian random variable $\mathcal{N}(0, \sigma^2)$.

A. Phase-Locked Loops

In a PLL-driven timing recovery architecture, the timing errors are corrected by changing the sampling instants $\boldsymbol{i}\boldsymbol{T}$ to $\boldsymbol{i}\boldsymbol{T} + \hat{\boldsymbol{\tau}}(\boldsymbol{i})$, where $\hat{\boldsymbol{\tau}}(\boldsymbol{i})$ are the estimated timing errors. These timing estimates are generated prior to the sampling instant $\boldsymbol{i}\boldsymbol{T}$ based on the past samples available from previously sampled data of the read-back signal. The corrected sampling process is given by

$$r(\boldsymbol{i}\boldsymbol{T} + \hat{\boldsymbol{\tau}}(\boldsymbol{i})) = d_{\boldsymbol{i}} h(\hat{\boldsymbol{\tau}}(\boldsymbol{i}) - \boldsymbol{\tau}(\boldsymbol{i})) + \sum_{\boldsymbol{k}\in\mathbb{Z}^2} d_{\boldsymbol{k}} h(\boldsymbol{i}\boldsymbol{T} - \boldsymbol{m}\boldsymbol{T} + \hat{\boldsymbol{\tau}}(\boldsymbol{k}) - \boldsymbol{\tau}(\boldsymbol{k})) + n(\boldsymbol{i}\boldsymbol{T} + \hat{\boldsymbol{\tau}}(\boldsymbol{i})). \tag{48}$$

The PLL-based timing architecture is shown in Fig. 19. This is a decision-directed scheme where an elementary form of the loop Viterbi detector is included to provide decision estimates on the individual bits. The reader must note that this loop Viterbi is a data-aided detector, and different from the signal detector before the ECC decoder in an iterative loop. The timing error detector (TED) is capable of using samples either in the form of the "preamble" (or "sync-mark") or from a 2-D signal detector depending on the mode of operation. The PLL operates in two modes: 1) the acquisition mode to train the PLL, which uses data from the preamble; and 2) the tracking mode which uses estimated decision information from the detector. The estimated error components $\hat{e}_x$ and $\hat{e}_y$ are filtered using a loop filter. The sampling at the $\boldsymbol{i}$th instant is done with the estimated timing offsets along x- and y-directions, using the components of $\hat{\boldsymbol{\tau}}(\boldsymbol{i})$. The PLL update is a combination of a 2-D digital equivalent of a 1-D voltage-controlled oscillator

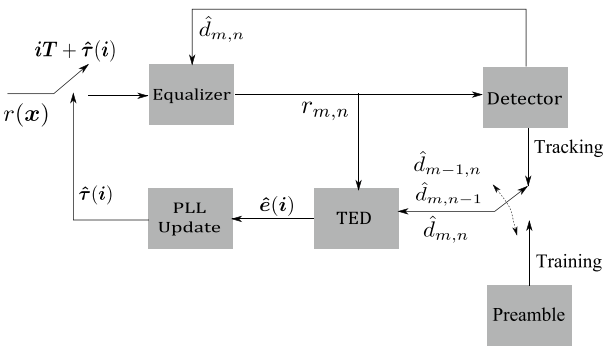


Fig. 19. ***Architecture of the 2-D PLL. The timing estimates $\hat{\tau}(i)$ are used to correct the sampling instants at $i^T T$ [92].***

(VCO) and a low-pass filter also known as a loop filter (LF) for noise rejection.

1) Timing Error Detector: The TED used in the 2-D PLL is capable of generating phase error estimates at every sample based on the current and past sampled values $r_{m,n}$, $r_{m-1,n}$, and $r_{m,n-1}$ and the corresponding decisions on these samples. For this, we bring in the notion of signal geometry into the update equations, extending the ideas of [93] naturally to a 2-D setting. Consider a vector of received samples $\vec{R}_{\boldsymbol{i}} = r_{m,n}\vec{i} + r_{m-1,n}\vec{j} + r_{m,n-1}\vec{k}$, where $\vec{i}$, $\vec{j}$, and $\vec{k}$ are unit orthonormal vectors in a 3-D space. Similarly, a corresponding decision vector $\vec{D}_{\boldsymbol{i}} = \hat{d}_{m,n}\vec{i} + \hat{d}_{m-1,n}\vec{j} + \hat{d}_{m,n-1}\vec{k}$ is formulated. To achieve synchronization on a 2-D grid, the angle between the two vectors $\vec{R}$ and $\vec{D}$ must be minimized in a 3-D space. The angle between the two vectors at the $\boldsymbol{i}$th instant $\theta_{\boldsymbol{i}}$ is given by

$$\sin(\theta_{\boldsymbol{i}}) = \frac{\vec{R}_{\boldsymbol{i}} \times \vec{D}_{\boldsymbol{i}}}{|\vec{R}_{\boldsymbol{i}}||\vec{D}_{\boldsymbol{i}}|}\vec{n}. \tag{49}$$

For small angles, $\sin(\theta_{\boldsymbol{i}}) \approx \theta_{\boldsymbol{i}}$. Ignoring the denominator term in (49), we can minimize the square of the numerator. $\theta_{\boldsymbol{i}}$ can be written as

$$\begin{aligned}\theta_{\boldsymbol{i}}^2 \approx\ & (r_{m,n}\hat{d}_{m-1,n} - r_{m-1,n}\hat{d}_{m,n})^2 \\ & + (r_{m,n}\hat{d}_{m,n-1} - r_{m,n-1}\hat{d}_{m,n})^2 \\ & + (r_{m-1,n}\hat{d}_{m,n-1} - r_{m,n-1}\hat{d}_{m-1,n})^2. \end{aligned}\tag{50}$$

The minimization of θ would involve minimizing each individual term in (50). We now define the terms $\hat{e}_x(\boldsymbol{i})$, $\hat{e}_y(\boldsymbol{i})$, and $\hat{e}_{xy}(\boldsymbol{i})$ as

$$\hat{e}_x(\boldsymbol{i}) = r_{m,n}\hat{d}_{m-1,n} - r_{m-1,n}\hat{d}_{m,n} \tag{51}$$

$$\hat{e}_y(\boldsymbol{i}) = r_{m,n}\hat{d}_{m,n-1} - r_{m,n-1}\hat{d}_{m,n} \tag{52}$$

$$\hat{e}_{xy}(\boldsymbol{i}) = r_{m-1,n}\hat{d}_{m,n-1} - r_{m,n-1}\hat{d}_{m-1,n}. \tag{53}$$

Noting that the equalizer is placed before the TED, it can be shown that the term $\hat{e}_{xy}(\boldsymbol{i})$ can be expressed as a linear combination of $\hat{e}_x(\boldsymbol{i})$ and $\hat{e}_y(\boldsymbol{i})$. This simplifies the minimization of θ^2, since it is now sufficient to minimize $\hat{e}_x$ and $\hat{e}_y$. It is to be noted that these terms are similar to the well-known 1-D M&M TED proposed in [93]. Furthermore, it can be shown that $\hat{e}_x(\boldsymbol{i})$ and $\hat{e}_y(\boldsymbol{i})$ can be expressed as linear functions of the gradients of the timing errors along the x- and y-directions.

2) PLL Update Equations: The PLL update in Fig. 19 is a combination of a digital VCO and an LF. We consider a second-order 2-D PLL for tracking. The update equations are given by

$$\begin{aligned}\hat{\tau}_x(m+1,n+1) =\ & \hat{\tau}_x(m,n) + K_x^{(p)}\hat{e}_x(m,n) \\ & + K_x^{(ix)}\sum_{l=-\infty}^{m-1}\hat{e}_x(l,n) + K_y^{(ix)}\sum_{l=-\infty}^{n-1}\hat{e}_x(m,l)\end{aligned}\tag{54}$$

and

$$\begin{aligned}\hat{\tau}_y(m+1,n+1) =\ & \hat{\tau}_y(m,n) + K_y^{(p)}\hat{e}_y(m,n) \\ & + K_x^{(iy)}\sum_{l=-\infty}^{m-1}\hat{e}_y(l,n) + K_y^{(iy)}\sum_{l=-\infty}^{n-1}\hat{e}_y(m,l).\end{aligned}\tag{55}$$

Here, $K_x^{(p)}, K_y^{(p)}$ are the proportional constants used to scale the error estimates $\hat{e}_x$ and $\hat{e}_y$, respectively. $K_x^{(ix)}$ and $K_y^{(ix)}$ are the integral scaling factors associated with $\hat{e}_x$ along the x- and y-directions, respectively. Similarly, $K_x^{(iy)}$ and $K_y^{(iy)}$ are the integral scaling factors associated with $\hat{e}_y$ along the x- and y-directions, respectively.

B. Interpolative Timing Recovery

In TDMR channels, specially designed ADCs are needed along both the directions for the servo to be able to correct for the timing errors, requiring real-time control of oscillators in the timing loop, which is difficult for practical reasons. To overcome the above issues, a fully digital 2-D ITR algorithm is proposed in [92]. The ideas in [92] extend the work of [94] and its variants, practically used in all 1-D storage channels for timing recovery. The 2-D read-back signal is oversampled by a small amount along both directions. The oversampling requirement in 1-D magnetic storage systems is around 5%–10%. In 2-D, we would need the servo system to be accurate up to 5%–10% in both directions. To overcome high phase errors, one can increase bit widths along the y-direction to allow greater inaccuracies of the read-head positioning system. This negatively impacts the channel-bit densities (CBDs). However, this enables us to isolate the head positioning system from the timing recovery algorithm using the ITR scheme described in this section.

The ITR architecture [94] and its variants are the state-of-the-art architecture in almost all 1-D storage channels. The ITR architecture [92], [95] for a batch-processing-based TDMR system is shown in Fig. 20.

The PLL is part of the timing recovery scheme. However, the interpolation mechanism provides more refined estimates of the desired sampling point instead of requiring an ADC or a servo to latch on to a sampling point

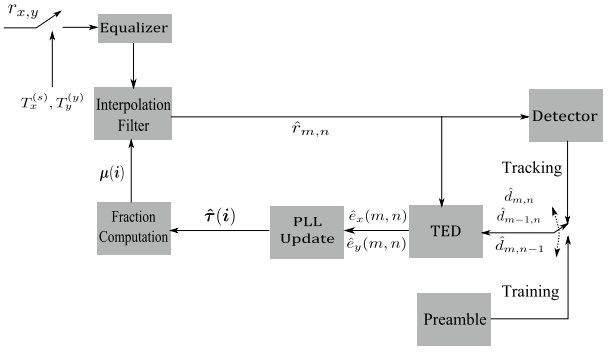


Fig. 20. ***Schematic architecture of the 2-D ITR scheme [96].***

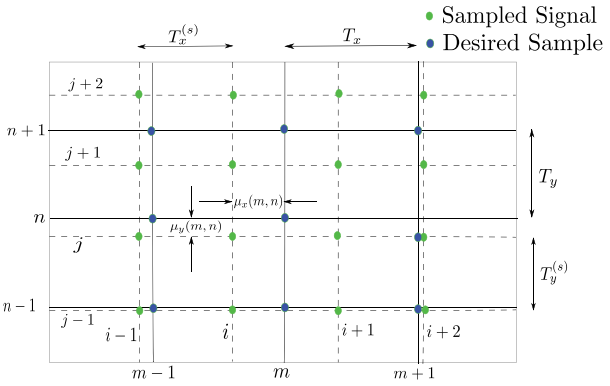


Fig. 21. ***The sampled points of the read-back signal j_TTs and the desired samples are at the intersections of the dotted and solid lines. The interpolation filter attempts to estimate the samples at the desired points from the sampled signal.***

by oversampling and interpolating the timing estimates. Fig. 21 illustrates the idea. The derivation of an optimal interpolation filter toward timing recovery based on the MMSE criterion is given in [95].

The 2-D ITR approach is demonstrated to provide superior gains in both timing estimates and implementation complexity for a fixed filter order compared to the sinc-based interpolation approach proposed in [92], paving the way for circuit realizations of this architecture.

C. Joint Timing and Detection

The 2-D PLL and ITR schemes discussed so far are still suboptimal in terms of the overall bit error rate performance at the output of the detector since the timing loop is decoupled from the signal detection engine. Also, the optimization criterion for the ITR timing recovery and the signal detection engines are different since the former is based on MMSE and the latter is based on ML/MAP. It is intuitive to fuse the timing engine with a near 2-D MAP performance signal detector, such as the joint self-iterating 2-D equalizer and detector [97], or the 2-D version of the soft output Viterbi algorithm (SOVA) detector [27] which is computationally less complex than the detector in [97], and then optimize the overall system for improved bit error rate performance.

There are other 2-D detectors, such as the GBP-based detector that are competitively optimal in performance to the detector in [97]. However, the GBP-based detector is impractical from implementation perspective due to high computational complexity. Recently, there has also been research towards realizing the detection algorithms in practice. Datta and Garani [98] have realized the VLSI design architecture of an efficient 2-D separable iterative soft output Viterbi detector on FPGA. An asynchronous version of the 1D Viterbi detector using 66.6% less power than the synchronous detector and sustaining a throughput of 2.4 Gbps has been conceived over a 65 nm technology by Dey et al. [99]. These design architectures can pave way for realizing the algorithms into actual circuits within a read channels IC for next generation of TDMR channels.

A full treatment of the 2-D signal detection problem for ISI channels is a self-contained topic in itself, beyond the scope of the current paper. We have briefly mentioned some of the key 2-D signal detectors in this section applicable to TDMR systems.

In order to conceive the joint 2-D timing recovery and signal detection [96], the timing errors have to be first discretized as shown in Fig. 22 and included within the definition of a trellis that operates over the joint state space of timing errors and 2-D channel ISI. In reality, the TDMR channel is nonlinear and time varying, and the channel conditions are not the same across all the zones on a magnetic disk. To allow controlled 2-D ISI, generalized partial response equalization

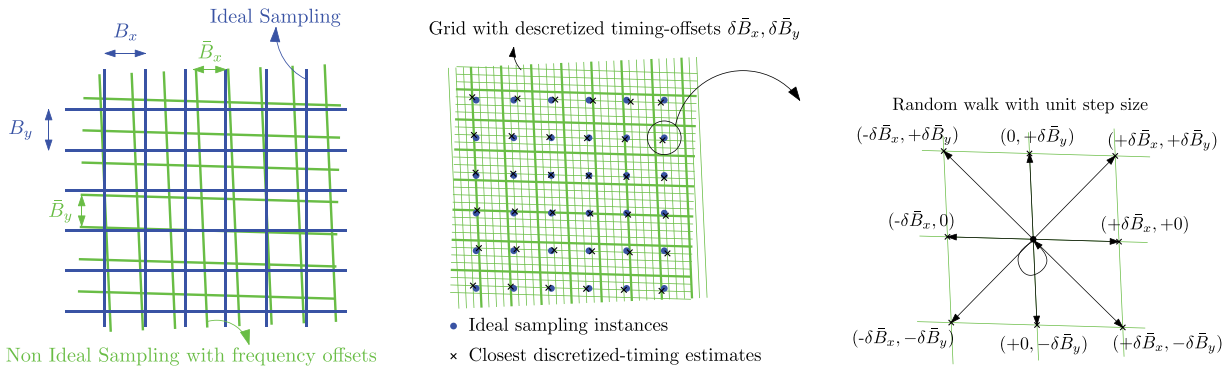


Fig. 22. ***Samples are oversampled and read back from the nonideal locations, including frequency offsets. Timing-error offsets are discretized using a finer grid for estimating the ideal-sampling location. The ideal-sampling location is estimated by minimizing ML metric over a possible finite discrete set of timing-error offsets [97]. (a) Grids corresponding to ideal sampling and non-ideal sampling with frequency offsets. The samples are oversampled during reading. (b) Timing error offsets are discretized according to a desired level of timing error resolution needed for estimating the ideal sampling location. The discretized timing estimates closest to ideal-sampling locations are shown. (c) This discrete set of timing-error offsets that include timing jitter can modeled as a 2D random walk process. The figure shows a 2D Random walk with a unit step in all the nine position accouting for diagonal drifts as well.***

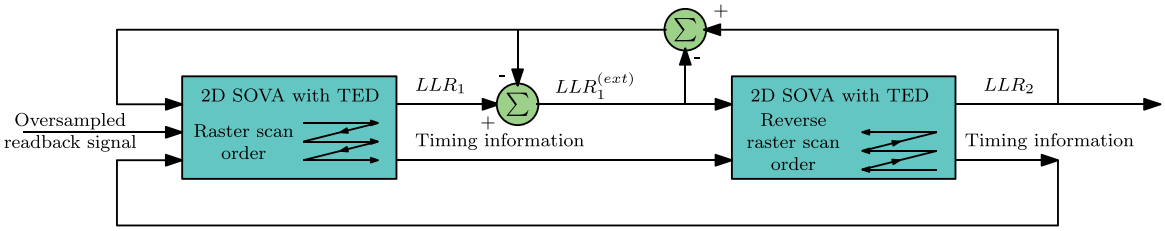


Fig. 23. ***Turbo scheme for 2-D joint timing recovery and signal detection. The scheme uses two instances of the joint timing detection algorithm, where one instance operates in the raster scan order, and the other instance operates in the reverse raster scan order. The two instances exchange timing information, as well as extrinsic information to achieve overall improvements in bit error rate performance [97].***

[27] must be done after a first pass of timing recovery using PLLs/ITR. Two-dimensional partial response targets could be separable or nonseparable [27] depending upon 1) the signal detection scheme; and 2) the desired extent of 2-D channel ISI, mindful of the tradeoff between SNR performance gain and implementation complexity. The 2-D channel ISI information along with the timing error model as shown in Fig. 22(c) must be included into the definition of a joint state space toward joint timing recovery and detection. The reader must note that this approach can naturally handle correlated timing errors along with signal detection within a Markov framework [96]. The likelihood probability is then computed over a local span of read-back samples. The timing errors are estimated along with the bit decisions by maximizing the likelihood probability as derived in [96].

The core engine in the joint timing and detection scheme is the 2-D SOVA that operates on a 2-D page of read-back data in the raster scan order. Due to the raster order of operation, the timing error estimates of future samples are not available to estimate the timing error at the current location. However, these estimates are available and get refined over the turbo iterative process.

Fig. 23 shows an iterative joint timing detector scheme where two instances of the proposed algorithm operate in a turbo loop.

The key ideas of the 2-D joint timing detection engine are summarized as follows.

1) The frequency offsets are first estimated during a training phase using a preamble of a 2-D sector.
2) The timing errors during the testing phase are modeled as discrete offsets from the sampled locations.
3) For each possible timing error of a current sample, the ideal sample is estimated using linear interpolation filters.
4) The estimated ideal samples are equalized using a PR equalizer.
5) The equalized samples are used to compute the ML metric corresponding to each possible data pattern and the timing-error offset.
6) The timing-error offset that minimizes the ML metric gives the estimate of the timing-error for the current sample.
7) The data pattern corresponding to the minimum ML metric provides the hard decision at the current location. The log-likelihood ratio for a bit are computed by the minimizing ML metric over all choices of inputs and by computing the alternative ML path with the bit flipped for the same timing error estimate and inputs.
8) Soft decisions are exchanged within a turbo loop.

It is reported that nearly 10% areal density gains can be realized using the iterative joint timing detector engine around the 1-Tb/in^2 regime with grain sizes of 10 nm and bit sizes of 25 × 25 nm at the output of 2-D soft output Viterbi algorithm (SOVA) as compared to a standalone timing loop coupled to a 2-D detector in an open-loop configuration over TDMR configurations comprising of a 2-D generalized partial response (GPR) equalization along the 2-D SOVA with data-dependent noise prediction (DDNP) capability over the Voronoi media model. Overall, with a full blown TDMR configuration, using innovations from signal detection, equalization and timing recovery, and error-correcting codes, the areal densities can be approximately doubled.

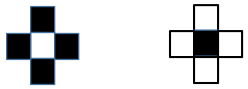
This concludes the discussion of full blown 2-D signal processing algorithms for TDMR. Next, we consider error-correcting code design along with other TDMR channel specific considerations for the design of these codes. We also survey some practical coding architectures that are part of the digital back end of the decoding circuitry in read channel integrated circuits (ICs.)

VI. CODE DESIGN AND OPTIMIZATION

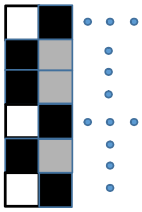
In this section, we describe error-correcting codes appropriate for TDMR systems. We begin with a discussion of modulation codes that enable useful constraints. Afterwards, we introduce graph-based codes, including the popular LDPC class of codes. The latter part of this section is concerned with practical LDPC architectures.

A. Modulation Codes

When grain sizes in TDMR systems approach bit sizes (1 b/grain), media noise becomes predominant, resulting in significant SNR degradation. Media noise occurs due to polarity changes in the magnetic flux of neighboring grains in



(a) 2D n.i.b. constraints



(b) 2D hard square constraints

Fig. 24. ***Configurations of some 2-D modulation constraints. (a) 3 × 3 n.i.b constraints juxtaposed side by side with a base pattern and its complement. (b) Two-dimensional (1, ∞) RLL constraint: The white and black squares indicate a "+1" and "−1," while a gray square can be either "+1" or "−1." The bits are populated within the array with the above constraints.***

a medium in response to input data transitions. Restricting these transitions is one of the important modulation constraints for TDMR. Two-dimensional transition limited constraints are typically low pass in nature [100]. Also, other modulation constraints, such as the 2-D runlength-limited (RLL) constraint [101], [102], and the checker board constraint [103] e.g., the no-isolated bit (n.i.b.) constraint are useful for TDMR channels to mitigate the effects of 2-D ISI. Modulation codes are mostly nonlinear codes with encoders that could be either fixed or variable rate. Fig. 24(a) and (b) shows various 2-D constraints applicable to TDMR.

Since the state space of the signal detector can be significantly pruned by not allowing certain transitions, the computational complexity of a 2-D ISI detector can be drastically reduced, facilitating the realization of the algorithm in silicon. The benefits of using modulation codes come at the price of code rate penalty. However, this tradeoff is part of TDMR system design, balancing the operating SNR at a desired areal density point, as well as facilitating reduced complexity signal detection by meeting the hardware design specifications of the read channel.

In earlier versions of hard disk drives that used peak detection circuits (d,k) RLL codes along with Reed–Solomon (RS)-based error-correcting codes were mainly used to boost areal densities. The d constraint was used for handling 1-D ISI, and the k constraint was used for timing recovery. By using PRML-based high-performance soft-output Viterbi detectors in the state-of-the-art PMR drives, the role of modulation codes is mainly restricted to timing, i.e., high rate ≈ 0.98 $(0, k)$ RLL codes are used. To design rate-efficient modulation codes, we need to compute the noiseless capacity of such input constrained channels. Using digraphs [104] or equivalent combinatorial representations [105], we can compute the capacity of 1-D constrained codes

Table 2 Two-Dimensional Modulation Constraint, Capacity Bounds/ Estimates, and Encoders for TDMR

2D constraint	Capacity estimates	Remarks on encoding
2D n.i.b	0.9238	variable rate [100]
$(1,\infty)$ **RLL**	0.5878	fixed and var. rate [110]
Low pass constr. [99]	$0.25 \leq C_{2D} \leq 0.67$	fixed rate

using well-known tools from symbolic dynamics and coding [104]. Also, there are algorithms for systematically constructing 1-D modulation codes, such as, for example, using the state splitting algorithm [106] and using fixed rate constructions derived from variable rate bit-stuffing techniques [107] to approach as close to capacity as desired.

The 2-D-noiseless capacity of constrained channels is defined as

$$C_{2-D} = \lim_{N\to\infty} \frac{\log_2(Z(N,N))}{N^2} \tag{56}$$

where $Z(N,N)$ is the 2-D partition function specifying the number of 2-D $N \times N$ arrays satisfying the modulation constraint.

Unlike the 1-D case, there is no systematic theory for computing C_{2-D}. Capacity bounds for 2-D RLL and checker board constraints have been computed using bit-stuffing techniques [101], [102] and by bounding the asymptotic estimate of the largest eigenvalue of the adjacency matrix of a 2-D constraint using finite length arrays [103], [108]. More recently, the GBP algorithm, described earlier in the Section III-E on channel modeling, has been successfully used for computing 2-D channel capacity estimates with reasonable approximation accuracy. In the GBP formulation, we can obtain the 2-D partition function by applying the GBP algorithm to the factor graph of $N \times N$ variable nodes with local constraints. Since the Helmholtz free energy is $F_H = \ln(Z)$, computing Z can be done by obtaining the region-based free energy estimate based on the beliefs for each region [109], [110].

Table 2 provides a summary of various 2-D constraints relevant to TDMR systems along with their bounds/estimates on the noiseless 2-D channel capacities and remarks on coding schemes. Most of the state-of-the-art coding schemes are variable rate with the exception of a few that are fixed rate [111].

Based on empirical evidence from error events collected post signal detection using the Voronoi-based channel model, it is found that the n.i.b. constraint is the dominant error event [110], [112]. To achieve the same storage density for a constrained coded system and an uncoded system, the rate loss due to the constrained input arrays must be compensated for by scaling the bit size of the coded system by a factor of R_c, which is the rate of the constrained code. This reduction in bit size is justifiable if the gain in the performance due to 2-D constrained coding is high enough to compensate for the effects of increased 2-D ISI. Therefore, the choice of the constrained code is dependent on the parameters of the TDMR system along with the signal detector. In [110], several TDMR system configurations are

Table 3 RSCT (RSDT) Denotes the Reader Response Span in Cross-Track (Down-Track) Dimension. CTC Is Assumed to Be 7 nm. All the Parameters in the Table Are Specified in Nanometers. ⋆ Indicates That the Parameter Is Varied in the Simulations

	TW	BP	RS_{CT}	RS_{DT}	TW_{50}	PW_{50}
TDMR(1)	⋆	7.5	30	21	20	14
TDMR(2)	⋆	7	30	21	20	14

evaluated. Table 3 shows the various parameters chosen at realistic physical values differing in the bit dimensions.

As we can observe from Fig. 25, we can get an improvement in the bit error rate using the modulation codes than without it over various TDMR system configurations. These benefits of constrained coding are seen at higher SNRs.

B. Graphical Codes

LDPC codes have found widespread use in a number of practical applications due to their excellent performance and low-complexity implementations. LDPC codes are represented by a sparse bipartite graph, where one set of nodes corresponds to coded bits (called variable nodes) and the other set of nodes, called parity-check nodes, represents the set of parity-check equations that the codewords must satisfy; see Fig. 26. Codes in which all variable nodes (check nodes) have the same degree are called regular, otherwise they are called irregular. Decoding of noisy bits can be efficiently performed using message-passing decoding algorithms in which messages are exchanged between variable and check nodes in an iterative fashion. Conceptually speaking, the message generation and exchange proceeds as follows. Based on messages received from their neighboring check nodes (Fig. 26, right red) and the input from the channel (Fig. 26, green), variable nodes update their values, and send out new messages to their neighbors (Fig. 26, right blue).

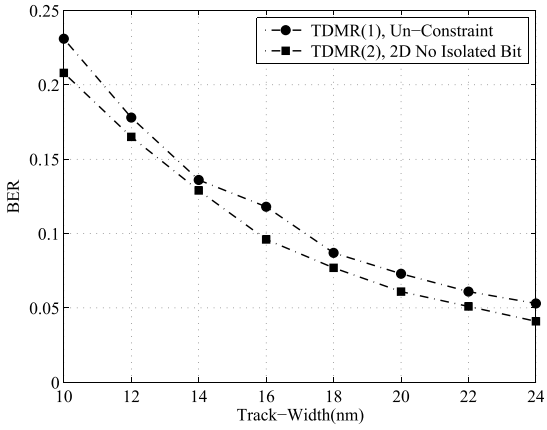


Fig. 25. *BER comparison of uncoded [TDMR(1)] and coded [TDMR(2)] systems with different bit areas and the same storage density in absence of electronic noise. Constrained coding improves the performance by avoiding the data patterns that result in high media noise.*

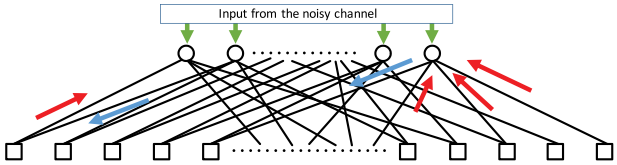


Fig. 26. *A bipartite graph representation of an LDPC code. Variable nodes are marked in circles and check nodes are marked in squares. A check node is satisfied if the mod 2 sum of its neighboring variable nodes is 0.*

In turn, check nodes evaluate whether they are satisfied with the updated values, and send the new set of messages to their neighbors, shown as left blue and left red in Fig. 26. The decoding terminates when either all parity checks are satisfied, i.e., when a codeword is reached, or when a maximum number of iterations is realized.

Binary LDPC codes are codes in which coded information is represented in terms of bits, and parity-check constraints operate on bits as well. More generally, nonbinary LDPC codes represent information in terms of symbols, wherein each symbol is a group of bits of some fixed size, and the associated parity-check equations are expressed in terms of resultant symbols. Typically, these symbols are drawn from some finite field of size 2^m, $m \geq 1$, so that m bits are grouped together to form a symbol.

Despite the early research focus on binary LDPC codes, it was empirically shown that nonbinary LDPC codes can significantly outperform their binary counterparts. Nonbinary LDPC codes are ideally suited for PR channels that require very low frame error rates (FERs). The key challenge is how to design an LDPC code that would offer best performance under ultra-stringent reliability constraints imposed in the PR systems.

It is well known empirically that LDPC codes perform well in a variety of practical applications. Recent results on integrating known LDPC codes into TDMR systems already indicate that LDPC codes are an excellent fit for future MR applications: TDMR systems incorporating existing binary LDPC codes were recently proposed in [13], [14], and [113]–[117], and those incorporating nonbinary LDPC codes were the subject of [118]–[120]. While the focus in these works is primarily on dealing with the other signal processing challenges discussed earlier, and not necessarily on the coding component, they nonetheless demonstrate the benefits of LDPC codes as the ECC scheme of choice.

Unlike in conventional communication systems with memoryless, AWGN noise, in TDMR there is an inherent difficulty in LDPC code design, due to the presence of the outer looping between the detector and the decoder. This additional looping can affect the messages passed between variable and check nodes inside the iterative decoder. EXIT chart analysis is a popular technique for LDPC code design [121], which constructs irregular codes with degree distribution that would have the best decoding thresholds (decoding threshold is an information-theoretic measure of how much

noise the code can tolerate and still be able to recover from errors [122]). Even though this approach is intrinsically asymptotic, it is customary to use it for the design of practical codes as well. When applied to the TDMR setting, due to the aforementioned outer looping, the EXIT chart approach must be used with care. Works in [123] and [124] develop LDPC codes specifically for the TDMR applications using the EXIT chart approach. The work in [124] also makes an interesting observation: when used in TDMR, LDPC codes with the degree distribution optimized using EXIT charts for AWGN setting perform considerably worse than the LDPC codes explicitly optimized for TDMR.

Another key property of TDMR—and other storage applications—is that they must operate under ultratight reli ability requirements. It is helpful to have analytical evalua tion tools so that channel coding components can be devel oped in a principled approach and deployed in practice with confidence. Vast literature exists on the theoretical characterization of the asymptotic performance of LDPC codes [122], [125]. While these results offer valuable goalposts, they are not readily translatable to the finite-length setting in which practical systems, notably including PR channels, must operate. In the asymptotic setting (where the EXIT chart approach operates), one assumes that the bipartite graph on which the code is defined is sufficiently cycle free, so that the decoding of noisy data can be performed exactly, using low-complexity, iterative algorithms. In contrast, in the finite-length case, idiosyncrasies associated with performing iterative decoding on graphs with cycles explicitly affect the performance.

The key challenge in designing good LDPC codes for practical channels is overcoming the so-called "error floor," a phenomenon in which the coding gains rapidly diminish even as the channel quality (measured in terms of SNR) increases; see Fig. 28 for illustration.

The error floor effect is caused by the presence of certain detrimental configurations in the graphical representation of the code. These configurations are vying with the codewords to be the output of the iterative decoder. Examples of such configurations are shown in Fig. 27. Notation (a, b) refers to the subgraph in the bipartite representation of the code that has a erroneous variable nodes and b unsatisfied check nodes. A codeword is then a $(c, 0)$ configuration, for some c. What is particularly fascinating is that these detrimental configurations can have weights a smaller than the minimum distance of the code. Thus, conventional approaches to code design based on optimizing for large minimum distance do not suffice in practical LDPC-coded systems. Substantial research has been devoted to understanding these structures in the canonical settings that encompass simple, memoryless channels with AWGN impairments (and their even simpler relatives, BEC and BSC), [126]–[129]. It thus might be tempting to simply export LDPC codes known to perform well over AWGN-like channels and use them in the PR systems [130]–[133].

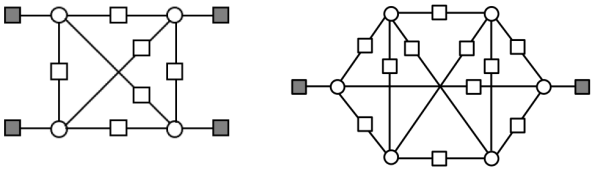


Fig. 27. ***(Left) (4, 4) configuration. (Right) (6, 2) configuration. Circles denote variable nodes and squares denote check nodes. When the shown variable nodes are set to 1 (and all other variable nodes are set to 0), white checks are the satisfied checks, and black checks are the unsatisfied checks.***

While this approach may offer some coding gains, we argue that much more can be accomplished if the channel code is designed in a channel-aware way. Intriguingly, the type of graphical configurations that are detrimental for LDPC-coded PR systems is fundamentally different from those that matter in the AWGN-like setting. This difference is primarily caused by the presence of memory in the PR channel. In the PR receivers, the detector and the decoder iteratively exchange their outputs for the benefit of both. A new input at the decoder is generated based on the updated information at the detector. This new input may cause the values of some of the variable nodes to be updated as well. With a sufficient number of outer iterations between the detector and the decoder, certain decoding errors can be prevented. As it turns out, these resolvable decoding errors are precisely caused by the configurations that dominate the error floor in the AWGN-like setting; the end result is that the type of detrimental configurations that matter in the PR systems is different than in the AWGN-like case.

Fig. 27 shows an example of two configurations that typically exist in the bipartite representation of a code with variable-node degree equal to 4 (and girth equal to 6). The configuration on the left is (4, 4) and the configuration on the right is (6, 2). For transmission over the AWGN channel for high enough SNR, if a decoding error occurs, the decoder most frequently gets stuck in a (4, 4) configuration. This is the

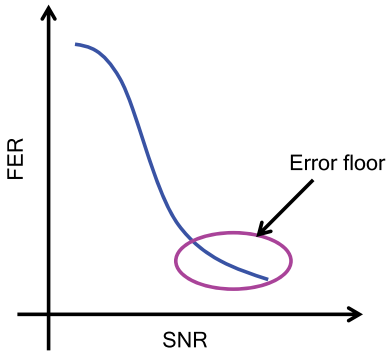


Fig. 28. ***Illustration of the "error floor" behavior of LDPC codes. Initially, as the SNR increases, there is a sharp downward slope as the FER decreases. However, this slope eventually levels off, leading to much smaller improvement in FER for high SNRs.***

smallest problematic configuration for which incorrect values of these four variable nodes cannot be overturned: for each variable node, three adjacent checks are in favor of the incorrect value and only one is opposed. The one check node is not powerful enough to overturn the consensus of the other three nodes. As a result, once the decoder enters the region of convergence around this object, it essentially remains in it forever (or, in practice, until the maximum number of iterations is reached). In contrast, for a PR channel and sufficiently high SNR, this type of error does get corrected: new information stemming from the outer detector/decoder looping is typically enough to tip the scales toward the correct variable node values, and the decoder "escapes" the (4, 4) configuration. In contrast, a (6, 2) configuration has a different ratio of satisfied and unsatisfied check nodes; it takes more effort to escape it. As a result, this configuration accounts for the majority of errors in the error floor regime in the PR setting.

The following example illustrates the benefits of channel-aware code design [134]. We simulate an exemplar of a regular LDPC code with the variable node degree of 4. The considered code has length 8178 bits and rate 0.82, and is defined over GF(4). The code has a parity-check matrix that is organized as a 2-D array of circulants, a preferred structure in practical implementations. By careful manipulation of edge weights and connections, it is possible to optimize such a code to ensure the non-existence of problematic con figurations, while maintaining the block-circulant struc ture (cf., [135]). Code optimization for AWGN-like chan nels amounts to the elimination of (4, 4) configurations, whereas, for the PR system one seeks to eliminate (6, 2) configurations. Fig. 29 shows that such code optimization yields considerable benefits—performance improvements in the FER is up to 2.5 orders of magnitude over the uninformed designs and over 1 order of magnitude over previous state-of-the-art results (curves marked in black); label "Fang" refers to [133] and label "Zhong" refers to [132]. The results further confirm that AWGN-optimized codes are inadequate for the PR systems [132].

There are several possible extensions to this approach. First, other types of high-performance graph-based codes can be designed in a channel-aware way. Spatially coupled (SC) codes are a recently proposed family of graph-based codes. They can be viewed as a chained version of individual LDPC codes, akin to the organization of convolutional codes, but now with the "convolution" operating on LDPC codes as constituents [136]. While the available results on SC codes are mostly focused on the asymptotic regime [137], benefits of using SC codes in practical settings are apparent as well. In fact, the added degree of freedom afforded by spatial coupling can be deftly exploited in a channel-aware way in the PR setting: it was recently shown that the parameter governing how the adjacent block LDPC codes are chained together can be optimized in such a way that the number of detrimental configurations in the error floor is minimized, which in turn maximizes the performance [138].

Polar codes are another recently proposed coding technique that achieves capacity in the limit of very large block lengths [139]. Making them practical (both in terms of complexity and code lengths) in realistic data communication and storage scenarios while maintaining excellent performance is a challenging endeavor that has recently become an active area of research. In the context of PR channels, it was recently shown in [140] that, when used in a multi-stage PR decoder architecture [141], properly designed polar codes can have good performance. A related result in [142] designed polar codes for ISI channels, and provided another independent confirmation that such codes outperform AWGN-designed codes when used over ISI channel. The work in [143] developed low complexity decoders for polar codes for PR channels; substantial reduction in complexity was achieved at the mild cost in performance relative to LDPC-coded PR systems.

In this section, we summarized recent research progress in coding for PR channels. These encouraging results can serve as a basis for a future study of channel codes, which, as several unrelated works independently point out [124], [134], [142], should be done in a channel-aware way. It would be particularly interesting to investigate multidimensional constructs that have planar constraints reflective of the intratrack and intertrack dependencies.

Computing the miscorrection error rates and accurately predicting the error floors for a given Tanner graph are important problems of continued theoretical and practical interest in storage channels. These metrics can help in predicting the coded system reliability. Good codes with miscorrection rates below 10^{-20} can obviate the need for any outer error detection codes, thereby improving the format efficiency even further.

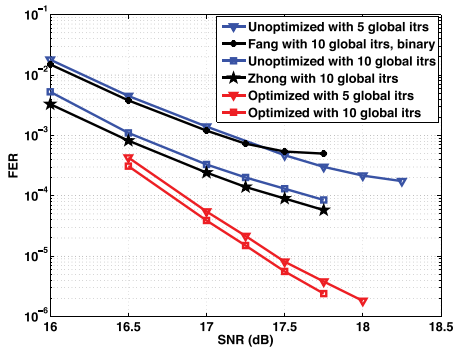


Fig. 29. ***Performance advantage of using a code optimized for the PR setting (see [133]).***

C. Other Channel Considerations

Storage channels impose other important considerations for ECC design. These include the ability to resolve burst erasures due to thermal asperities and media defects [144]. Media defects can be either deep or shallow. Deep defects are usually spread over a smaller number of bits, while shallow defects are more wide spread [145]. In earlier versions of the track-based magnetic recording, burst erasures were

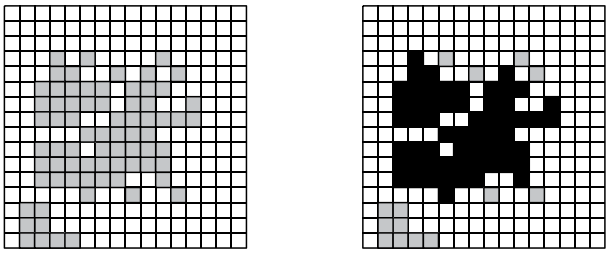


Fig. 30. ***Two-dimensional defective regions on a medium are identified within a largest edge connected region. These are later flagged as erasures and corrected using an LDPC code and a channel detector. (a) 2D defective regions. (b) Identified rectangular bursts.***

overcome by using RS codes in conjunction with inner iterative codes. Using post-ECC modeling techniques based on the block multinomial model [144] and hidden Markov models (HMMs) [147], [148], using data collected from critically failing drives, the t level error-correction power for an RS code was decided for the given media conditions.

Though RS codes can provide guaranteed error-correction ability, they are inferior in performance to carefully constructed structured LPDC codes that exhibit excellent performance in the waterfall and error floor regions along with good erasure-correction ability. Fossorier [149] provided a construction of LDPC codes that can achieve the Roger bound for hard decision decoding, i.e., an (n, k) LDPC code that can correct bursts up to a length of $n - k - 1$. Construction of LDPC codes for iteratively correcting burst erasures using the belief propagation algorithm by identifying trapping sets have also been investigated in [150] and [151]. Carefully designed interleavers can enhance the burst erasure capability of the LDPC code.

The identification of burst erasures is an important step toward error correction. Traditional approaches include using RLL codes, or a full response reequalization [152] for defect identification. Also, in the context of PMR channels, signal processing cues, such as low signal energy over a defective region, low LLR values observed at the output of a signal detector and signature analysis from frequently occurring state transitions within the trellis states of a signal detector state trellis over the defective region have been very successful to flag the onset of defects [153].

Defect detection for TDMR channels poses significant challenges since defective regions have arbitrary shapes and sizes that must be identified accurately, unlike the 1-D case with a linear geometry. Fig. 30(a) shows the defects on a 2-D medium. These defects can be irregularly shaped in 2-D, forming cluster errors. By identifying 3×3 squares that are defective and growing these squares over the defective region to accommodate all edge connected bit cells, Matcha and Srinivasa [112] were able to map most of the defective cells to form a largest edge connected region as shown in Fig. 30(b). Those cells that were not mapped as part of the region growing procedure were treated as random errors.

Fig. 31 shows the schematic of a defect detector burst erasure-correcting architecture using a 2-D SOVA detector and an LDPC decoder configured within a iterative turbo loop. The LLR values within the detector are always fixed to zero for defective cells to mark erasures. For other bits, the LLR values are populated using the extrinsic information from the decoder. The defect detection algorithm was able to correct 38×38 burst erasures, yielding more than 2-dB gain in electrical SNR. By using inter-codeword and intra-codeword interleaving schemes, up to 76×76 burst erasures were corrected [112]. The design of good interleavers [154] is also important for enhancing the burst erasure capability of the channel. Interleaving can add decoding latencies. Carefully embedding interleavers within the LPDC code [155] can provide zero latencies during decoding, significantly boosting the system performance.

Recently, Matcha *et al.* [156] have reported the construction of native 2-D LDPC codes for effectively handling 2-D burst erasures. They have also developed a 2-D joint detection decoding engine based on the GBP algorithm for TDMR channels. The 2-D LDPC code is shown to correct 20% more burst erasures compared to the 1-D LDPC code over a 128×256 2D page of detected bits, showing the direct benefits of native 2-D coding.

D. Practical LDPC Coding Architectures

Structured graphical codes devoid of harmful trapping sets are useful toward practical read channel coding architectures. Also, for storage systems, throughput, area, and

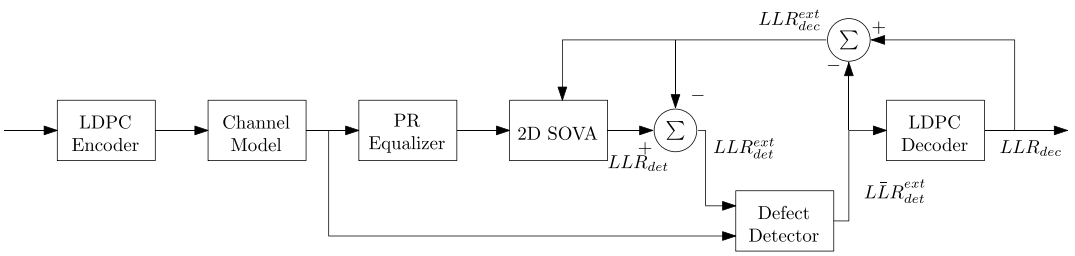


Fig. 31. ***Schematic of a defect detector and erasure decoder architecture for TDMR. The LLR values for bits identified as defects are set to zero in the channel detector. The LDPC decoder provides extrinsic information for these erasures. The detector and the decoder are iteratively configured to resolve the burst erasures.***

power are the factors that lead to difficulty in design as one would not prefer to reread, reencode, and rewrite back on the medium. The standard sum product algorithm (SPA) gives the best decoding performance. However, SPA is not favored in hardware due to logarithmic and multiplicative components within the check node unit. The min-sum algorithm (MSA), which is a simplification of SPA, is suited for hardware design due to its simplicity [157]. The traditional min-sum algorithm processes the block rows in parallel, leading to large area. A modified form of the MSA, called the layered MSA [158], [159], is the state-of-the-art algorithm used in virtually all practical LDPC decoders based on serial processing, yielding both SNR gains due to faster convergence as well as area efficiency over the traditional MSA at the cost of throughput.

In the layered MSA [160], the block columns and block rows are processed serially. Fig. 32 shows the block diagram of the decoder. The architecture consists of check node units (CNU), barrel shifters toward realizing the intended parallelism, adders, subtractors, and block random access memories (BRAMs) for storing the intermediate overall reliability information P, check node messages Q, and variable node messages R. The CNU array is composed of p parallel CNU units which compute the partial state for each row to produce the R messages in block serial form. The MUX is required to supply new LLRs to the decoder when the decoder has corrected the previous frame or the maximum iteration limit is reached. Normally, signed to 2's complement and 2's complement to signed converters are required before and after the CNU in case of uniform quantization.

The MUX at the input of the cyclic shifter takes care of the initialization for decoding a sector of data. In the beginning, the output of the R select unit is set to a zero vector.

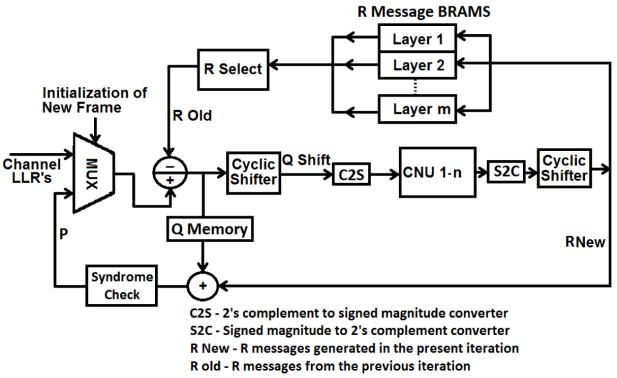


Fig. 32. ***Block diagram of the layered decoder.***

The P messages are computed by adding the delayed version of the Q messages (which are stored in BRAM until the serial CNU produces the output) to the R messages. The R messages are then stored in a R message BRAM, which would be used in subsequent iterations. The next block row is now ready to be processed as the P messages are directed by the MUX to the subtractor. The next block row is operated in a similar way as explained before. For the next iteration i (if the syndrome has not been satisfied for iteration $i-1$), the R select unit directs R messages from the previous iteration to the subtractor. The process goes on till the sector has been corrected, or a maximum iteration limit has been reached.

The check node unit [160] in Fig. 33 emulates the operations at the check node on a Tanner graph. It sends back the minimum of the values received from a certain variable node, discounting the variable node. The check node unit consists of a minimum value N_1 and a second minimum value N_2 finder, a partial state that stores N_1 and N_2 temporarily

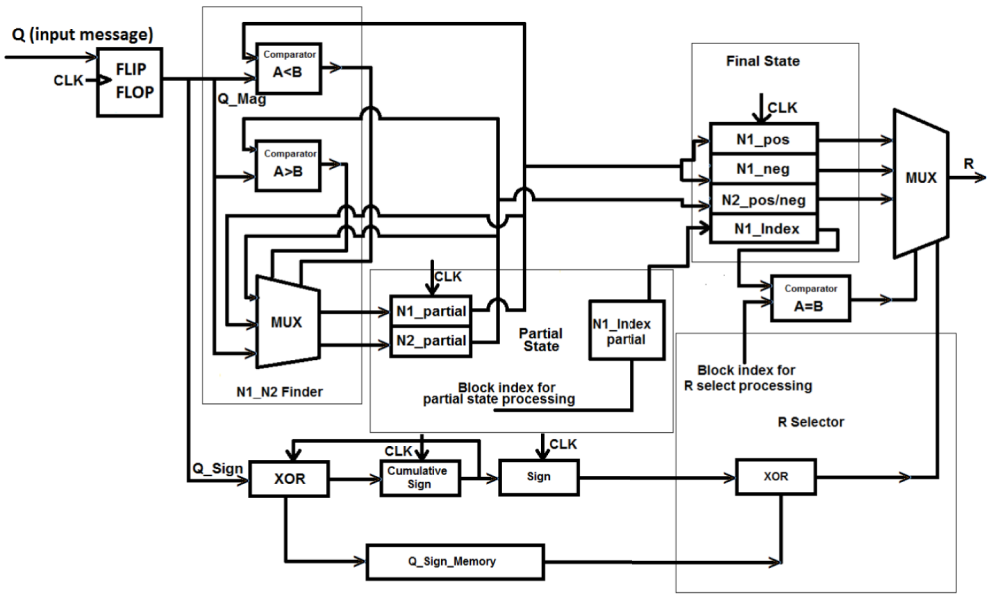


Fig. 33. ***Architecture of the CNU. Q and R represent the incoming and outgoing messages, respectively.***

and updates them on each clock cycle, a final state which stores the final N_1 and N_2 value, and a sign processing unit which takes care of the sign of the LLR to be sent. Incoming variable messages are compared to two up-to-date least minimum numbers to generate new partial state. In this state, we have N_1 (first minimum value), N_2 (second minimum value), and the index of N_1. The final state is achieved after all the messages have been received. The R selector then assigns one of these two values (N_1 and N_2) based on the index of N_1 and sign of all the R messages generated by the XOR logic.

Recently, Mondal *et al.* [161] have developed efficient coding architectures for RS and LDPC decoders. The technology-scaled normalized throughput of the pipelined RS decoder is almost two times compared with the existing decoders with an overall processing latency reduced by almost 80% compared with the existing designs. Also, nonuniform quantization is explored in LDPC decoding architecture yielding 20% area savings (using 1 b less) for the block RAMs used for storing intermediate check node and variable node messages. Since almost all iterative codes use an outer detection code (EDC), such as the RS code for guaranteed miscorrection performance, these architectures are useful toward practice.

To the best of our knowledge, most of the codes employed in shingled recording and early versions of TDMR are still based on 1-D LDPC decoders with various versions of 2-D signal processing (single and multiple tracks). Efficient architectures for decoding native 2-D codes, such as in [156], and variants would be of practical interest for applications in these systems. We also remark that the design of fast and efficient decoder hardware architectures can also help in semi-analytical approaches for predicting the performance of these graphical codes in the absence of a rigorous theory and exact analysis to assess code performance metrics.

VII. CONCLUSION AND PERSPECTIVES

In this work, we analyzed the promising new technology of TMDR. Unlike other proposed strategies to reach higher areal densities in magnetic storage (on the order of 10 Tb/in^2), TDMR does not require either radical changes and redesigns of the magnetic medium or the read/write heads. In fact, TDMR reuses these components from existing magnetic storage technologies, relying instead on shingled recording and vastly more powerful signal processing and coding algorithms to mitigate the resulting issues.

We discussed TDMR channel models, where we introduced a hierarchy of models, starting from simpler, lower complexity models that are less accurate, building up to more complex, but also more accurate models, such as the Voronoi media model (the model we focused on) and micromagnetic models. Capacity estimation and its application to areal density projection were also considered.

Afterwards, we introduced signal processing algorithms necessary for the functioning of TDMR systems. We introduced single-track and multitrack detection, including strategies for multitrack detection of asynchronous tracks. Furthermore, we examined timing recovery algorithms using 2-D PLLs leading toward a 2-D joint timing recovery and signal detection techniques applicable to true TDMR systems with native 2-D sectors, beyond current generation shingled systems.

Last, we provided an overview of error-correcting code design. Such codes fell into two classes: modulation codes that enable certain constraints in order to avoid problematic effects in TDMR, and graph-based codes, such as the prominent LDPC class of codes. Although LDPC codes have been studied and proposed for many applications over the last two decades, we considered the optimization of such codes specifically for the TMDR channel. Additionally, we discussed practical LDPC architectures.

Considering the timeliness and importance of TDMR in taking the next step forward in magnetic storage, we hope that our work provided a useful introduction to the numerous research challenges and novel solutions brought to light to advance this proposed technology.

Successful deployment of TDMR technology will bring in a significant changes in the way hardware and software systems at the operating system level would operate around this paradigm. With technology advancements from shingled recording toward a fully 2-D paradigm, one can expect significantly high throughput rates from these systems. This requires carefully engineered read channel architectures using parallel and distributed structures to reduce latencies during detection and decoding. The design of efficient low power architectures to realize the signal processing and coding techniques for TDMR would be quite challenging.

We hope that novel solutions conceived as a part of 2-D channels engineering to enable TDMR technology can find their way into other applications in physical layer communications and possibly rekindle channel engineering efforts for digital holography and 3-D imaging.

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ABOUT THE AUTHORS

Shayan Srinivasa Garani (Senior Member, IEEE) received the B.E. degree in electronics and communication engineering from Mysore University, India, the M.S degree in electrical engineering from the University of Florida, Gainesville, FL, USA, and the Ph.D. degree in electrical and computer engineering with a minor in mathematics from Georgia Institute of Technology, Atlanta, GA, USA.

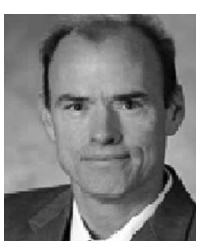
He is a faculty member within the Department of Electronic Systems Engineering, Indian Institute of Science (IISc), Bengaluru, India, where he directs the Physical Nano-memories, Signal, and Information Processing laboratory (PNSIL). Prior to joining academics, he was managing the advanced read channels division at Western Digital (USA), leading advanced research and development efforts on disruptive technologies that went into products, and directing several external university research programs. He was the Chairman for the Coding and Signal Processing group within IDEMA-ASTC and the Co-Chair for the overall technological committee. He is the author of a book, several journal and conference publications, holds a dozen U.S. patents and many others pending in the area of coding and signal processing for data storage. His research interests related to physical data storage include broad areas of information theory, coding and signal processing for emerging physical nanomemories and high-speed, low-power VLSI architectures for storage applications.

Dr. Garani is a Senior Member of the Optical Society of America. He currently serves as the Vice Chair (Academics) for the IEEE Data Storage Technical Committee.

Lara Dolecek received the B.S. (with honors), M.S. and Ph.D. degrees in electrical engineering and computer sciences, as well as the M.A. degree in statistics, all from the University of California Berkeley (UC Berkeley), Berkeley, CA, USA.

She is an Associate Professor at the Electrical Engineering Department, University of California Los Angeles (UCLA), Los Angeles, CA, USA. Prior to joining UCLA, she was a Postdoctoral Researcher at the Laboratory for Information and Decision Systems, Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. Her research interests span coding and information theory, graphical models, statistical algorithms, and computational methods, with applications to emerging systems for data storage, processing, and communication.

Prof. Dolecek received the 2007 David J. Sakrison Memorial Prize for the most outstanding doctoral research in the Department of Electrical Engineering and Computer Sciences at UC Berkeley. She received IBM Faculty Award (2014), Northrop Grumman Excellence in Teaching Award (2013), Intel Early Career Faculty Award (2013), University of California Faculty Development Award (2013), Okawa Research Grant (2013), NSF CAREER Award (2012), and Hellman Fellowship Award (2011). With her research group, she received the best paper award from IEEE Globecom 2015 conference. She currently serves as an Associate Editor for the IEEE Transactions on Communications.



John Barry (Senior Member, IEEE) received the B.S. degree (*summa cum laude*) from the State University of New York at Buffalo, Buffalo, NY, USA, in 1986 and the M.S. and Ph.D. degrees from the University of California at Berkeley (UC Berkeley), Berkeley, CA, USA, in 1987 and 1992, respectively, all in electrical engineering. His doctoral research explored the feasibility of broadband wireless communications using diffuse infrared radiation.

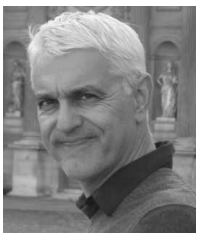
Since 1985, he has held engineering positions in the fields of communications and radar systems at Bell Communications Research, IBM T.J. Watson Research Center, Hughes Aircraft Company, and General Dynamics. He is a coauthor of *Digital Communication* (Norwell, MA, USA: Kluwer, 2004, 3rd ed.). He is a coeditor of *Advanced Optical Wireless Communication Systems* (Cambridge, U.K.: Cambridge Univ. Press, April 2012). He is the author of *Wireless Infrared Communications* (Norwell, MA, USA: Kluwer, 1994).

Dr. Barry received the 1992 David J. Griep Memorial Prize and the 1993 Eliahu Jury Award from UC Berkeley, a 1993 Research Initiation Award from the National Science Foundation (NSF), and a 1993 IBM Faculty Development Award. Currently, he serves as a Guest Editor for a special issue of the IEEE Journal on Selected Areas in Communications.

Frederic Sala received the B.S.E. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2010 and the M.S. and Ph.D. degrees in electrical engineering from the University of California Los Angeles (UCLA), Los Angeles, CA, USA, in 2013 and 2016, respectively.

He is a Postdoctoral Researcher in the Stanford InfoLab, Stanford, CA, USA. His research interests include machine learning, information theory, coding theory, and algorithms, with applications to data storage systems and data management.

Dr. Sala is a recipient of the National Science Foundation (NSF) Graduate Research Fellowship, the UCLA Edward K. Rice Outstanding Masters Student Award, and the UCLA EE 2016–2017 Outstanding Ph.D. Dissertation in Signals and Systems Award.



Bane Vasić (Fellow, IEEE) received the B.S., M.S., and Ph.D degrees in electrical engineering from the University of Niš, Niš, Serbia, in 1989, 1991, and 1994, respectively.

He is a Professor of Electrical and Computer Engineering and Mathematics at the University of Arizona, Tucson, AZ, USA and a Director of the Error Correction Laboratory. He is an inventor of the soft-error-event decoding algorithm, and the key architect of a detector/decoder for Bell Labs data storage read channel chips which were regarded as the best in industry. His pioneering work on structured LDPC error-correcting codes and invention of codes has enabled low-complexity iterative decoder implementations. Structured LDPC codes are today adopted in a number of communications standards and data storage systems. He is known for his theoretical work in error-correction coding theory and codes on graphs which has led to characterization of the hard decision iterative decoders of LDPC codes, and design of decoders with best error-floor performance known today. He is a cofounder of Codelucida Inc., a startup company developing advanced error-correction solutions for communications and data storage.

Dr. Vasić is a Fulbright Scholar, da Vinci Fellow, and a past Chair of the IEEE Data Storage Technical Committee.